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9	Ethernet Switch
10	Ethernet Ports
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14	Reset, RCW PLDs, Optional MCU
15	Clocking
16	TDM COVER
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Revisions			
C	Release for PCB Rev C to support P1020E.	May 2009	Austin HW
D	Fixed all outstanding errata (CE5 - CE16)	Jan 2010	Austin HW

RDB supporting P1020, P1011, P2020, P2010 Devices

Schematic is used for different P1 and P2 devices.
The DNPs shown in this schematic accommodate P1020.

NMG
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: FCP: ____ FIUO: PUBI: X

Designer: Austin HW	Drawing Title: RDB for P1 and P2 Devices	
Drawn by: Austin HW	Page Title: Cover and TOC	
Approved: Austin HW	Size: C	Document Number: SCH-26158 PDF: SPF-26158 Rev: D
	Date: Monday, February 01, 2010	Sheet 1 of 18

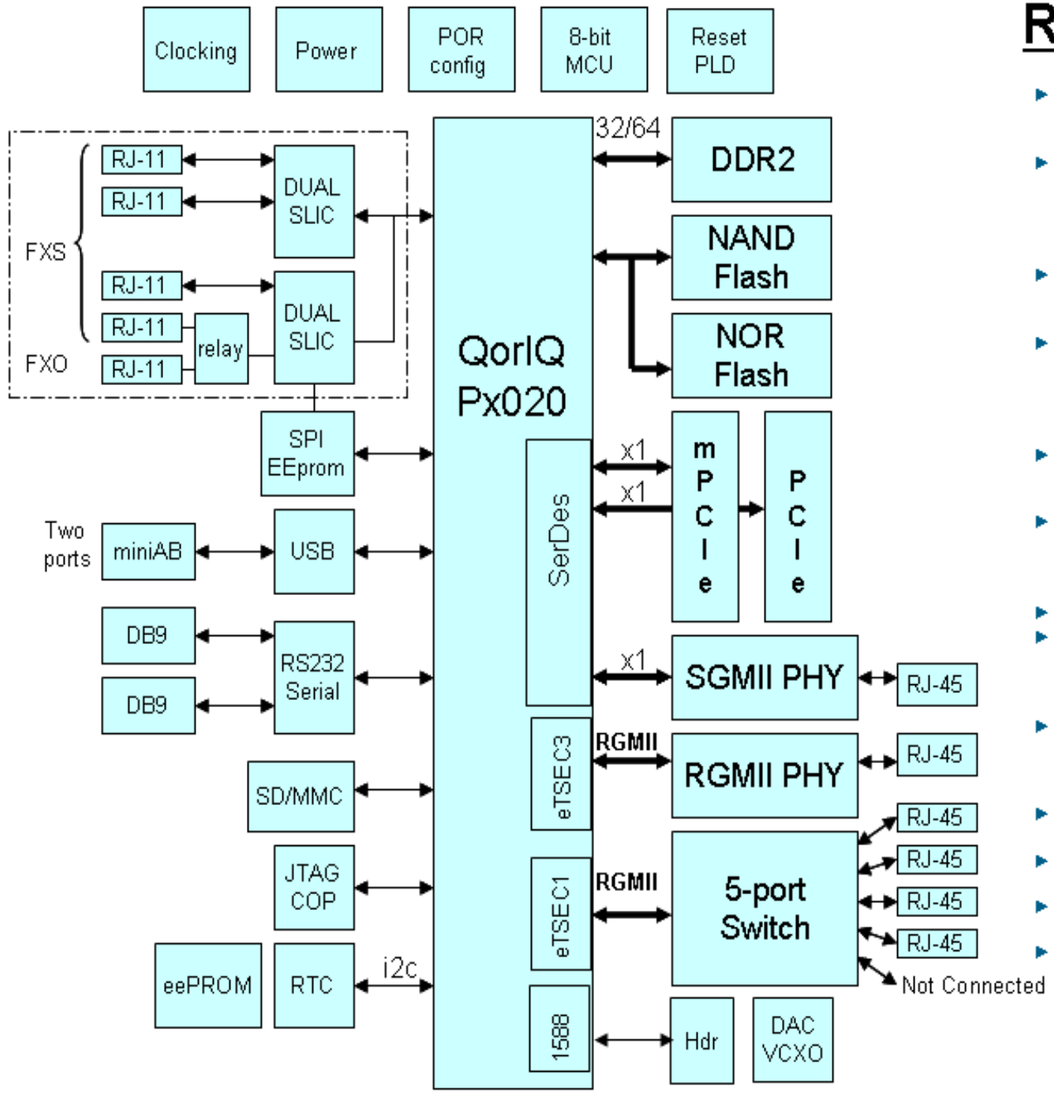
1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/8 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.



RDB Platform

- Common PCB supporting
  - P1020 @ 800 MHz core speed 0.95V
  - P2020 @ 1.2 GHz core speed 1.05V
- Memory
  - DDR2 – 512MB/1GB/2GB
  - NOR Flash – 16Mbyte (128Mbit device)
  - NAND Flash – 32MByte
  - SPI ROM – 16MByte
- PCIe
  - One standard PCIe connector (x1)
  - One mini PCIe connector (x1)
- Ethernet
  - Six 10/100/1000 ports as follows:
  - 4-ports from L2 switch connected to eTSEC1
  - 1 SGMII PHY connected to eTSEC2
  - 1 RGMII PHY connected to eTSEC3
- 1588
  - Clock input from DAC / VCXO circuitry
  - Accessible via test header
- I2C
  - Serial eePROM – boot loader
  - Serial eePROM – board identification
  - RTC
- SD/MMC card slot
- TDM
  - Support Legerity Dual SLIC
  - 4 FXS ports
  - 1 FXO port via relay
- USB
  - Option #1 -Two Mini AB connectors on IO Panel (default)
  - Option #2 –Two Type A connectors (front panel)
- MCU
  - 8-bit FSL microcontroller
- UARTs
  - Two DB9 connectors
- Form Factor
  - Mini-ITX chassis
- Schematics – OrCad; PCB - Allegro

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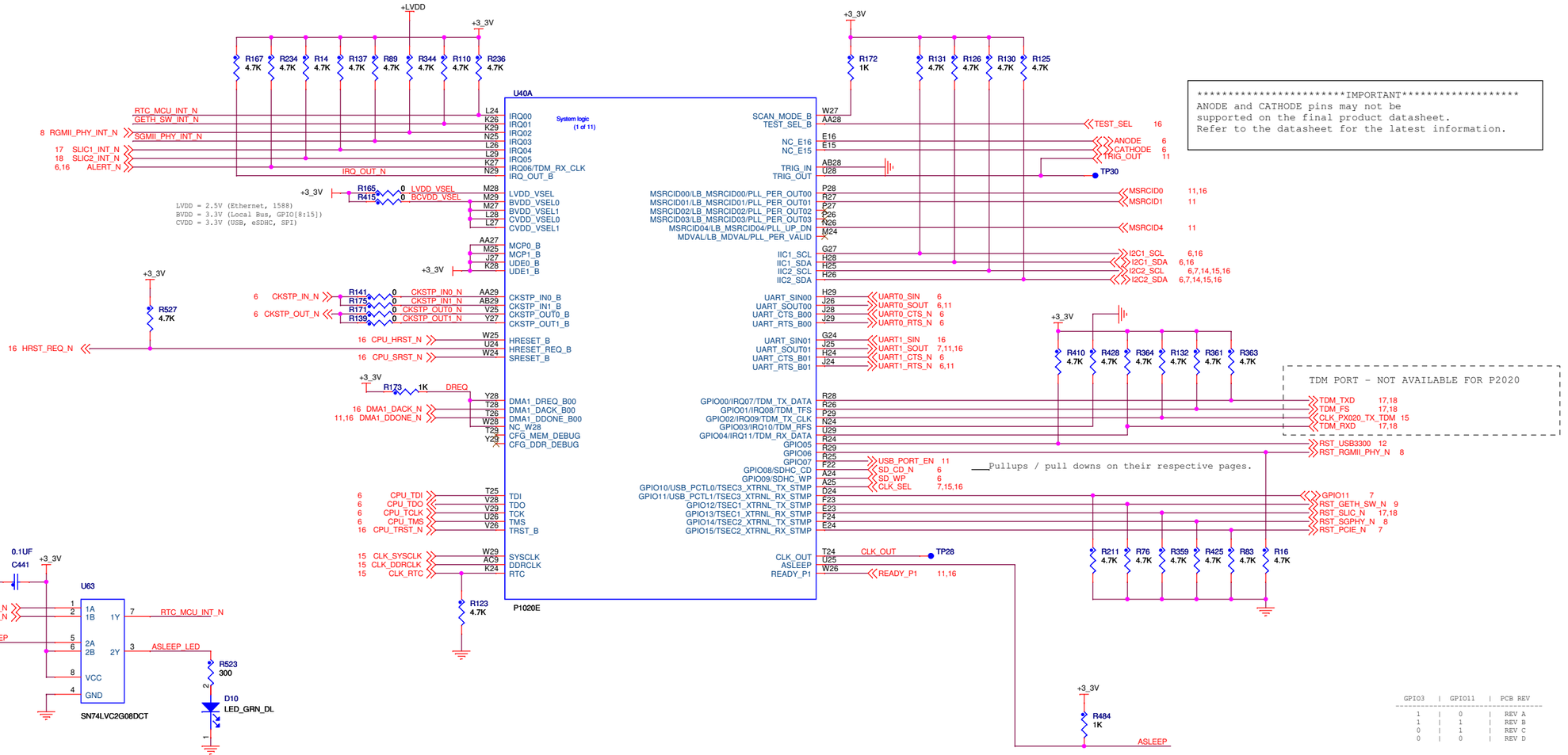
ICAP Classification: FCP:___ FIUO: PUBI: _x_

Drawing Title: **RDB for P1 and P2 devices**

Page Title: **Block Diagram**

Size	Document Number	Rev
C	SCH-26158 PDF: SPF-26158	D

Date: Monday, February 01, 2010 Sheet 2 of 18



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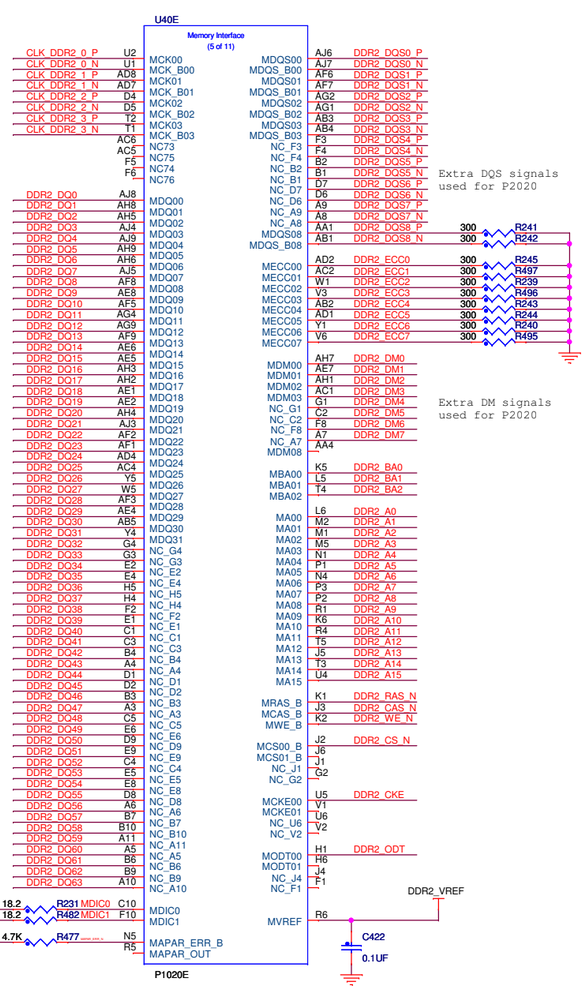
ICAP Classification: FCP: ___ FIUO: <FIUO> PUBI: X

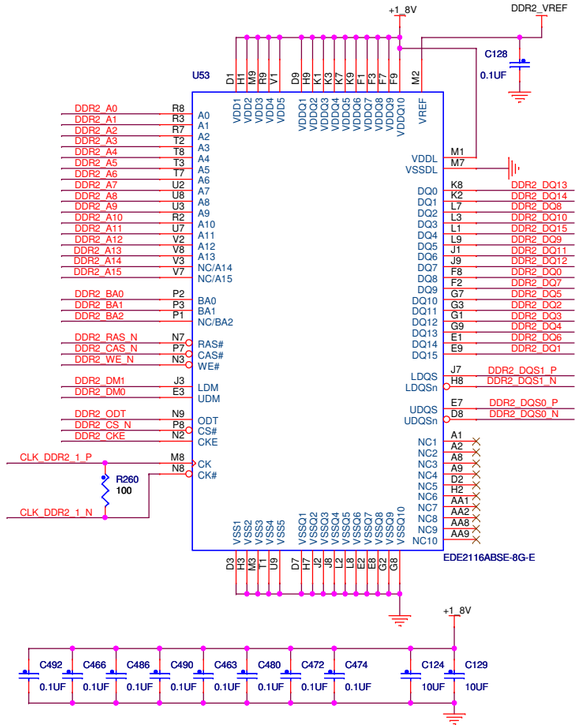
Drawing Title: **RDB for P1 and P2 devices**

Page Title: **CPU Misc**

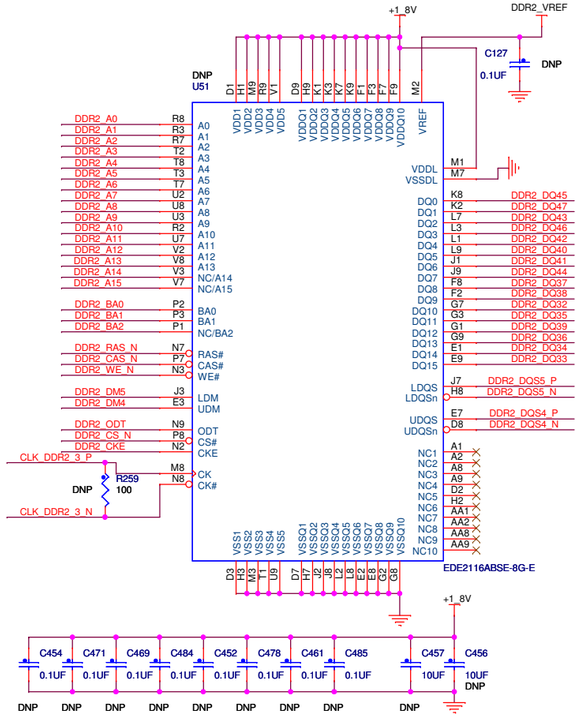
Size	Document Number	Rev
C	SCH-26158 PDF: SPF-26158	D

Date: Monday, February 01, 2010 Sheet 3 of 18





Bottom chips used when 64-bit interface support is needed. (i.e P2020). They are DNP for 32-bit devices such as the P1020 devices,



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ICAP Classification: FCP: ___ FIUO: <FIUO>PUBI: X

Drawing Title:

RDB for P1 and P2 devices

Page Title:

DDR2 Memory

Size	Document Number	Rev
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For P2020, all VDD pins are common for both single and dual core devices.

Populate for single core P10xx devices and remove CPU_VDD resistor.

Populate for single core P10xx devices and remove CPU_VDD resistor.

AVDD filter is for P2020. For P1020, the filter is not needed.

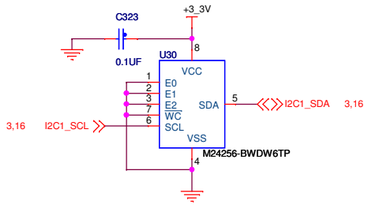
U40B Power (2 of 11) — P1020E

U40C Grounds (3 of 11) — P1020E

U40D Power/Misc (4 of 11) — P1020E

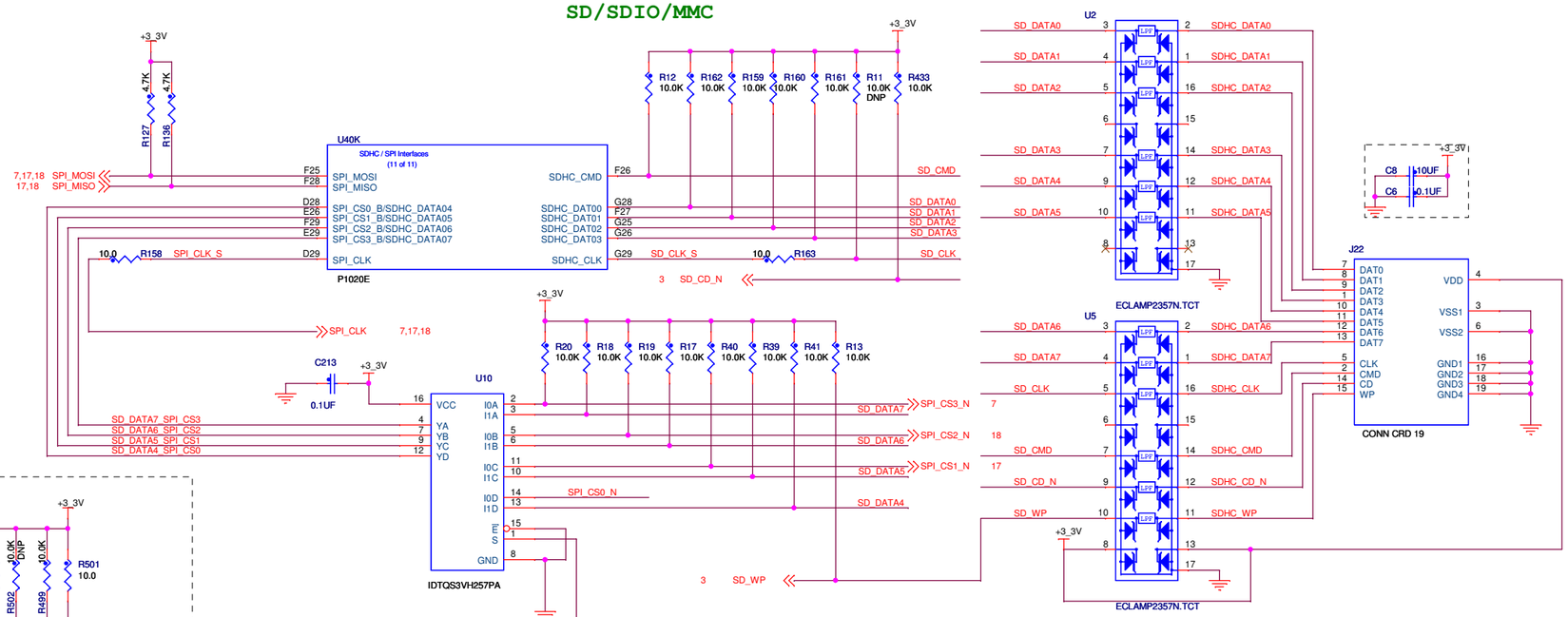
ICAP Classification:	FCP: ___ FIUO: <FIUO>PUBI: X
Drawing Title:	RDB for P1 and P2 devices
Page Title:	CPU Power and Ground
Size: C	Document Number: SCH-26158 PDF: SPF-26158 Rev: D
Date: Monday, February 01, 2010	Sheet 5 of 18

BOOT I2C1 EEPROM

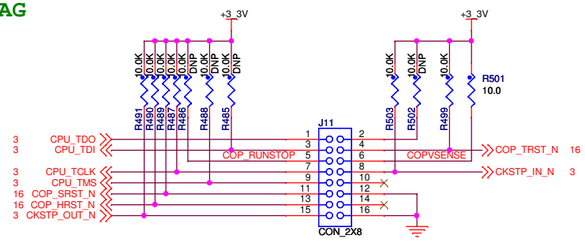


I2C1 ADDRESS:
"1010,A2,A1,A0" = 50H

SD/SDIO/MMC

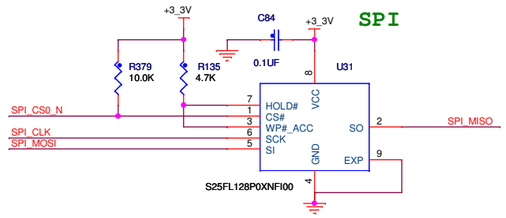


JTAG

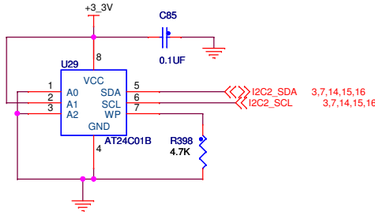


TCK pulled up by 5-10K
TMS pulled up by 5-10K
TDI pulled up by 5-10K
TRST# ANDed with PORESET#
COP pin 2 NC / short to GND
COP pin 5 (QREQ#) pulled up by 5-10K
COP pin 15 (CKSTP_OUT) pulled up by 5-10K
COP pin 6 connect to 3.3V by 1K for current limiting

SPI

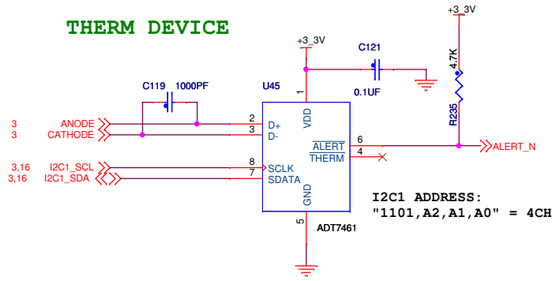


BRD EEPROM



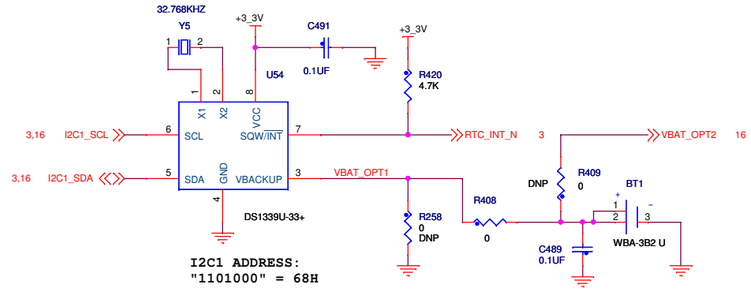
I2C2 ADDRESS:
"1010,A2,A1,A0" = 52H

THERM DEVICE



I2C1 ADDRESS:
"1101,A2,A1,A0" = 4CH

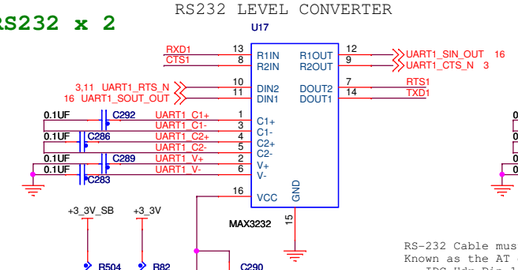
RTC



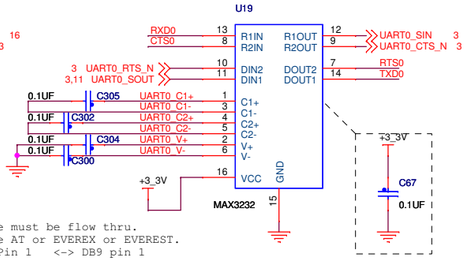
I2C1 ADDRESS:
"1101000" = 68H

RS232 x 2

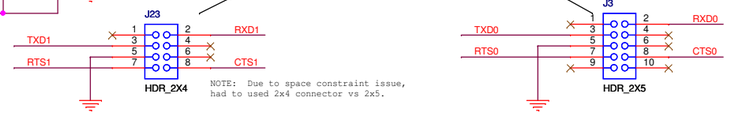
RS232 LEVEL CONVERTER



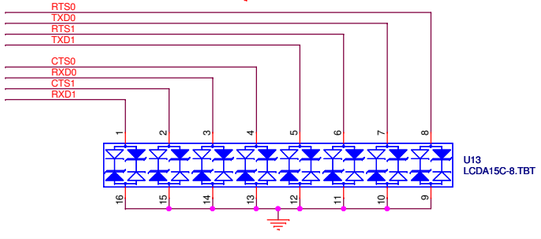
RS232 LEVEL CONVERTER



RS-232 Cable must be flow thru.
Known as the AT or EVEREX or EVEREST.
IDC Hdr Pin 1 <-> DB9 pin 1
.....
IDC Hdr Pin 9 <-> DB9 pin 9



NOTE: Due to space constraint issue, had to used 2x4 connector vs 2x5.



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ICAP Classification: FCP:___ FIUO: <FIUO>PUBI: X

Drawing Title: **RDB for P1 and P2 devices**

Page Title: **I2C, SPI, SD/MMC, JTAG, RS232, RTC**

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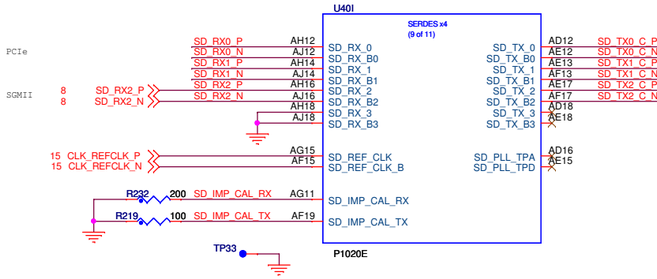
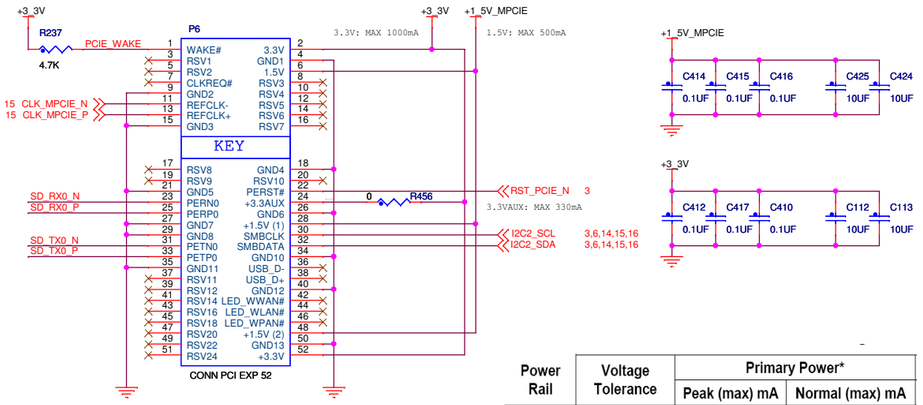
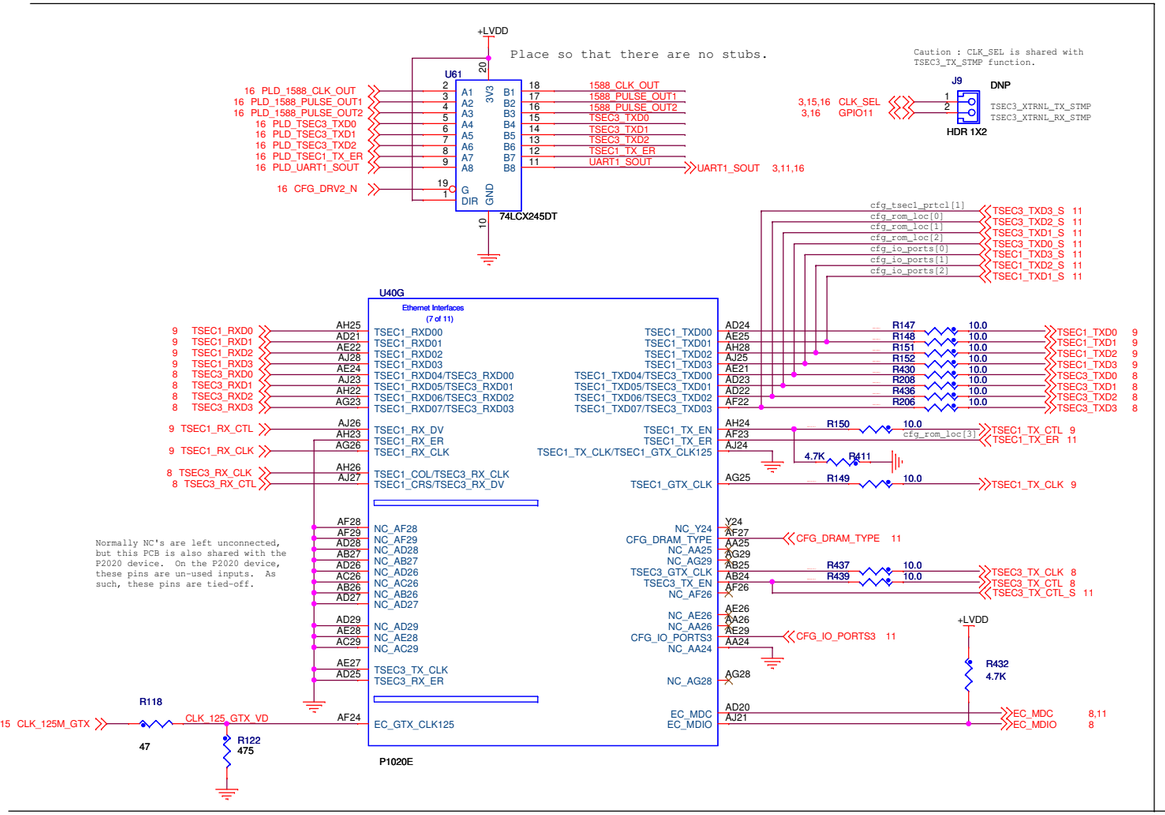
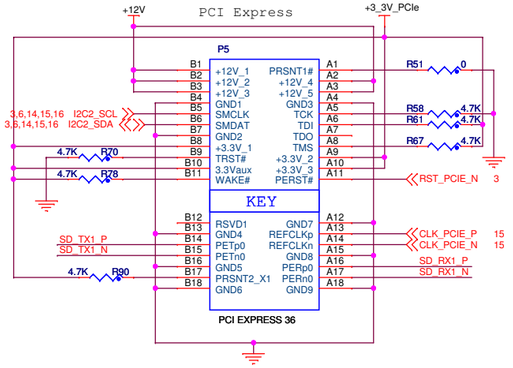


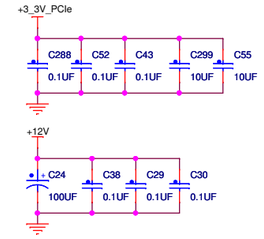


Mini PCI Express Connector

Power Rail	Voltage Tolerance	Primary Power*	
		Peak (max) mA	Normal (max) mA
+3.3V	±9%	1,000	750
3.3Vaux	±9%	330	250
+1.5V	±5%	500	375



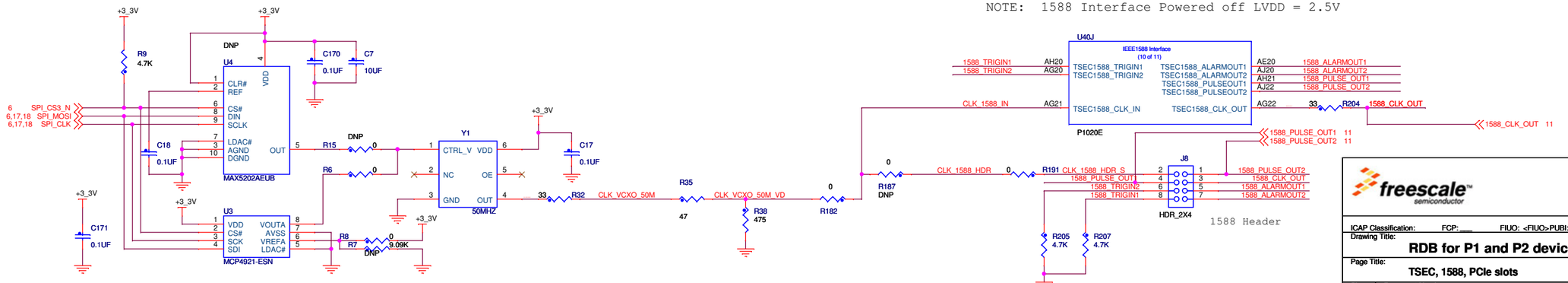




Power Rail	10 W Slot
+3.3V	
Voltage tolerance	± 9% (max)
Supply Current	3.0 A (max)
Capacitive Load	1000 μF (max)
+12V	
Voltage tolerance	± 8%
Supply Current	0.5 A (max)
Capacitive Load	300 μF (max)

IMPORTANT - x1 PCIe cards are rated as 10W are less.
As such, only x1 PCIe cards are allowed in this slot.
Secondly, the chassis supply can only support x1 PCIe cards.

NOTE: 1588 Interface Powered off LVDD = 2.5V



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ICAP Classification: FCP: ___ FIUO: <FIUO>-PUBI: X

Drawing Title:

RDB for P1 and P2 devices

Page Title:

TSEC, 1588, PCIe slots

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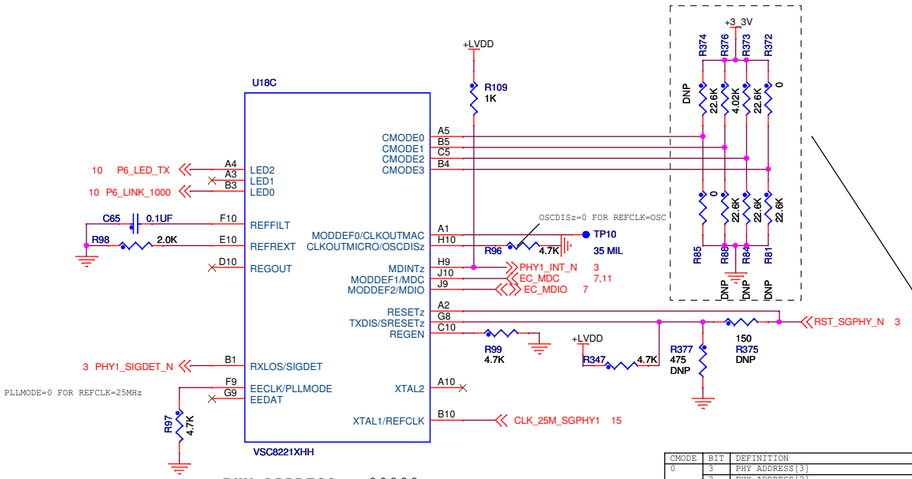
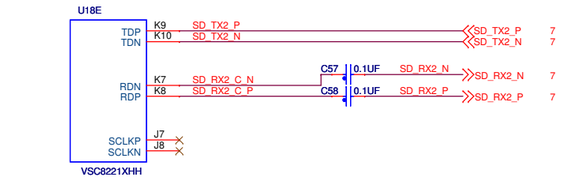
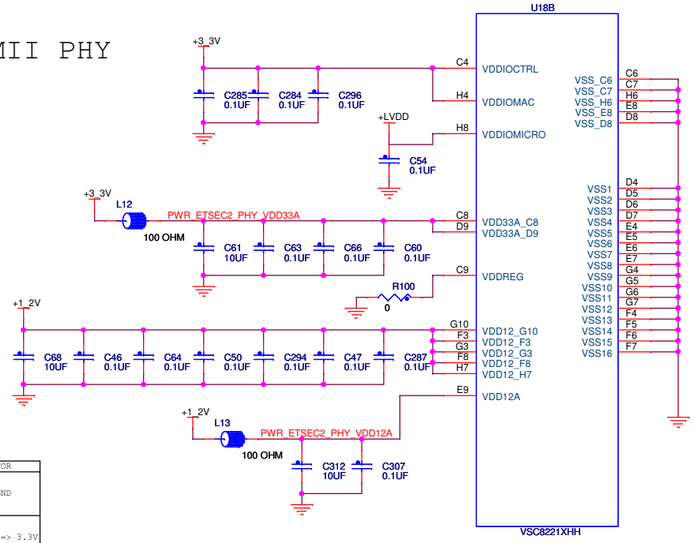
SGMII PHY

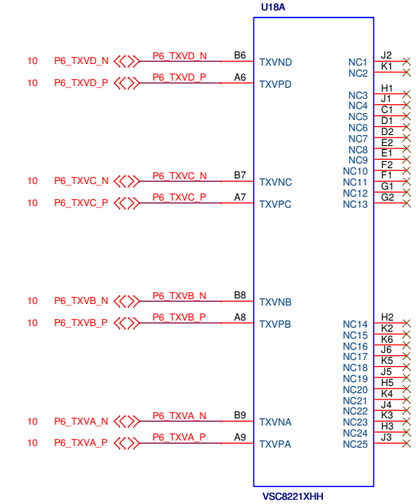


PHY ADDRESS = 00000

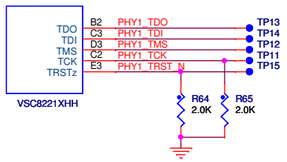
CMODE	BIT	DEFINITION	SET	RESISTOR
0	3	PHY ADDRESS[3]	0000	0 => GND
	2	PHY ADDRESS[2]		
	1	PHY ADDRESS[1]		
	0	PHY ADDRESS[0]		
1	3	SFP MODE DISABLE	1010	4.02K => 3.3V
	2	PHY ADDRESS[4]		
	1	SIGDET PIN DIRECTION		
	0	SERDES LINE IMPEDANCE		
2	3	PHY OPERATING MODE[3]	1111	22.6K => 3.3V
	2	PHY OPERATING MODE[2]		
	1	PHY OPERATING MODE[1]		
	0	PHY OPERATING MODE[0]		
3	3	LED CONTROL[1]	1000	0 => 3.3V
	2	SQE ENABLE		
	1	RESERVED		
	0	AUTO-NEGOTIATION ADVERTISEMENT CONTROL[1]		





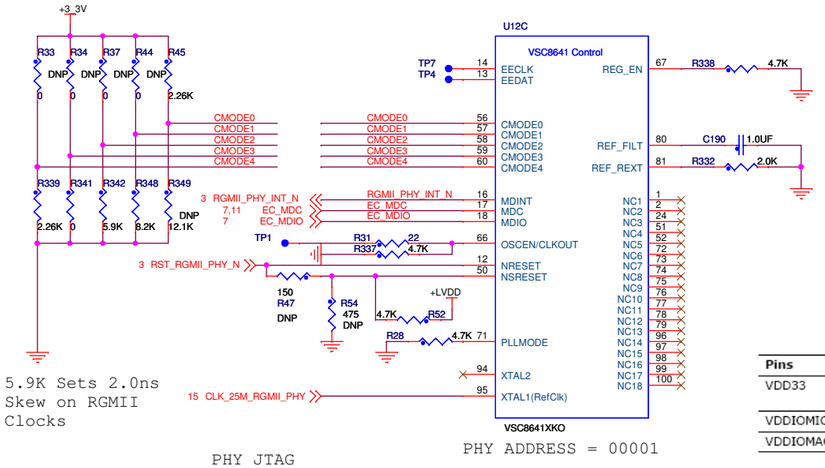


Power Supply Pins	Nominal Voltages	Associated Functional Pins
VDDIO	3.3V or 2.5V	RXLOS/SIGDET, MODDEF0/CLKOUT
VDDIO-MICRO	3.3V or 2.5V	EECLK/PLLMODE, EEDAT, TXDIS/SRESET, MDINT, MODDEF1/MDC, MODDEF2/MDIO, CLKOUTMICRO/OSCDIS
VDDIO-CTRL	3.3V or 2.5V	RESET, TDO, TDI, TMS, TCK, TRST
VDD33A	3.3V	LED[2:0], CMODE[3:0], TXVND, TXVPD, TXVNC, TXVPC, TXVNB, TXVPB, TXVNA, TXVPA, XTAL2, XTAL1/REFCLK, REFFILT, REFREXT
VDDREG	3.3v	REGOUT
VDD12	1.2V	RDP, RDN, TDP, TDN, SCLKP, SCLKN
VDD12A	1.2V	



RGMII PHY

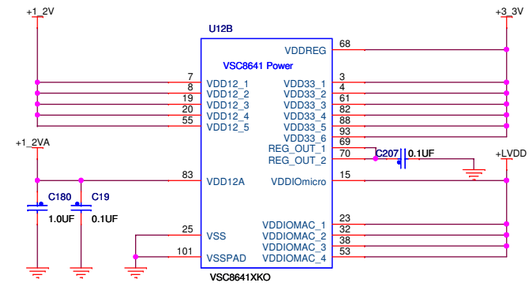
PHY CONTROL SIGNALS



5.9K Sets 2.0ns Skew on RGMII Clocks

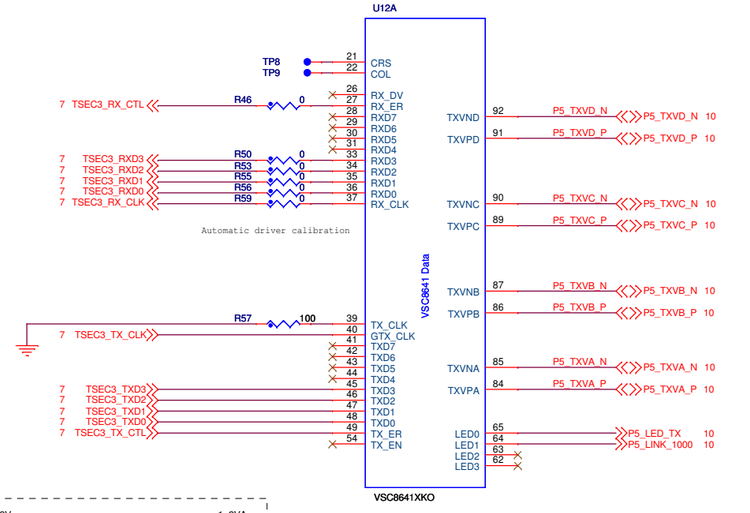
PHY ADDRESS = 00001

PHY POWER PINS

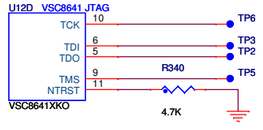


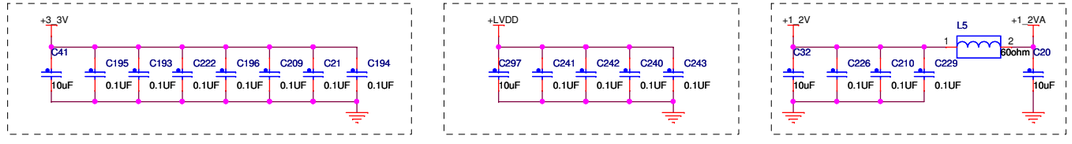
Pins	Nominal Voltage	Associated Functional Pins
VDD33	3.3 V	LED[2:0], CLKOUT, NRESET, JTAG (5), XTAL1, XTAL2, CMODE, TXVP, TXVN, REF_FILT, REF_REXT
VDDIOMICRO	2.5 V, 3.3 V	MDC, MDIO, MDINT, EECLK, EEDAT
VDDIOMAC	2.5 V, 3.3 V	RXD, RX_CTL, RX_CLK, TXD, TX_CTL, TX_CLK, NSRESET

RGMII MAC INTERFACE



PHY JTAG





ICAP Classification: FCP:___ FIUO: <FIUO>PUBI: X

Drawing Title: **RDB for P1 and P2 devices**

Page Title: **Ethernet Phys**

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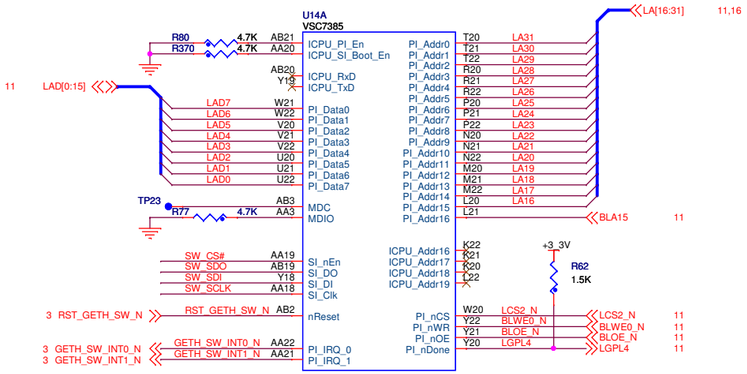
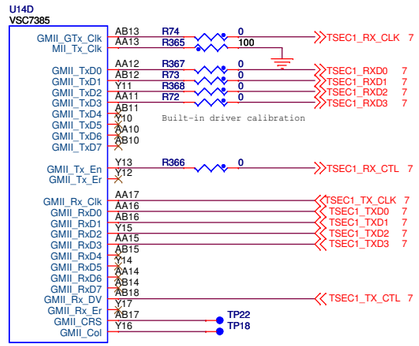
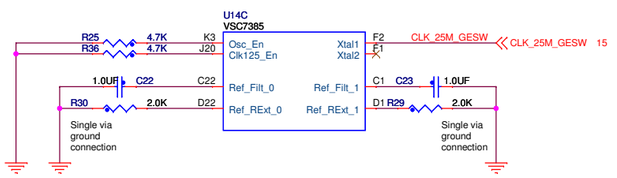
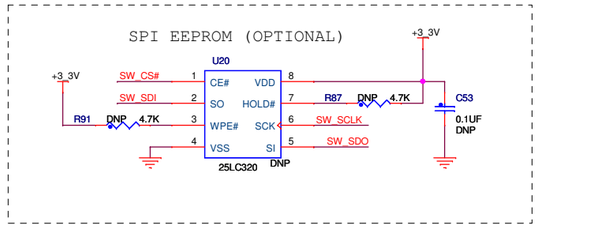
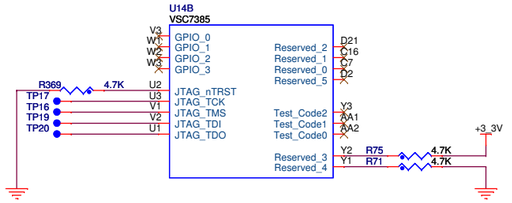
GIGABIT ETHERNET SWITCH INTERFACE
MAC INTERFACE SIGNALS



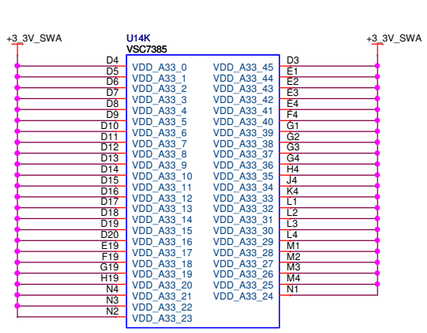


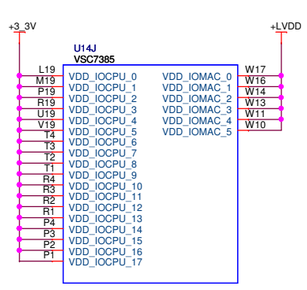


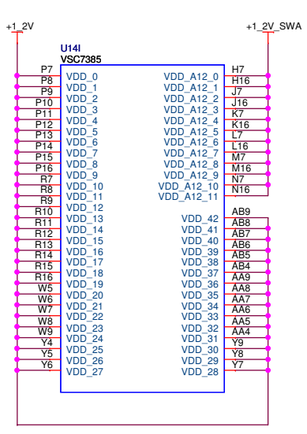


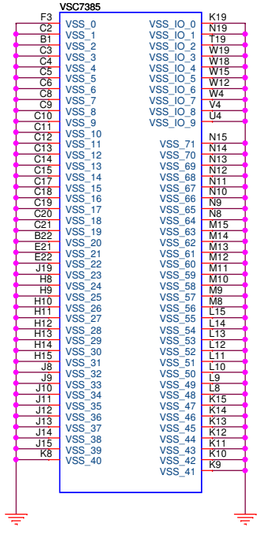


ETHERNET SWITCH POWER PINS



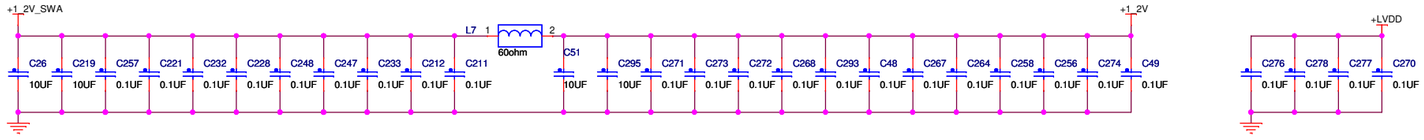


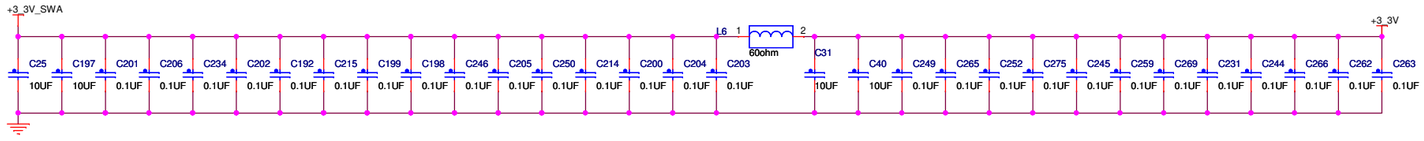




Power Supply Pins	Nominal Voltages	Associated Functional Pins
$VDDIO_{MAC}$	3.3V, 2.5V, 1.5V	TXD[3:0], TX_CTL, TX_CLK, RXD[3:0], RX_CTL, RX_CLK, TXREF_n, $CLK125_{MAC}$
$VDDIO_{micro}$	3.3V, 2.5V, 1.5V	SOFT_RESET, RESET, MDINT_n, MDIO, MDC, MICROREF, $CLK125_{micro}$
$VDDIO_{ctl}$	3.3V, 2.5V	TDI, TDO, TMS, TCK, TRST, EEDAT, EECLK
VDD33	3.3V	LED[4:0], CMODE[7:0], TXVN, TXVP, REF_REXT, REF_FILT, XTAL1

DECAPS FOR ETHERNET SWITCH





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ICAP Classification: FCP: ___ FIUO: <FIUO>PUBI: X

Drawing Title: **RDB for P1 and P2 devices**

Page Title: **Ethernet Switch**

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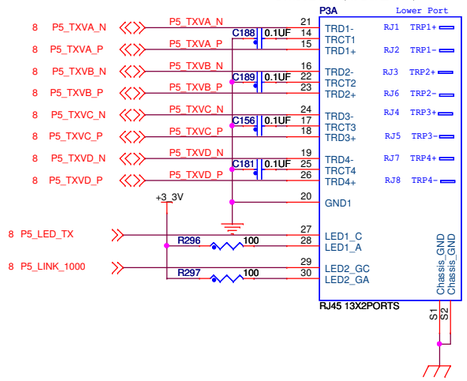
GIGABIT ETHERNET PORTS

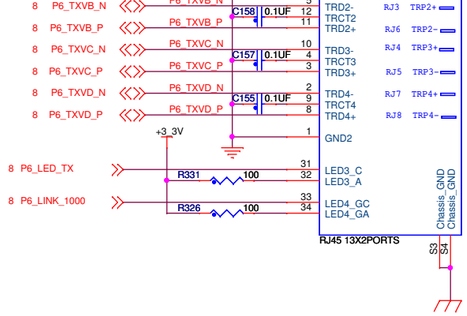
RGMII (eTSEC3) and SGMII (eTSEC2)

RGMII (eTSEC3)

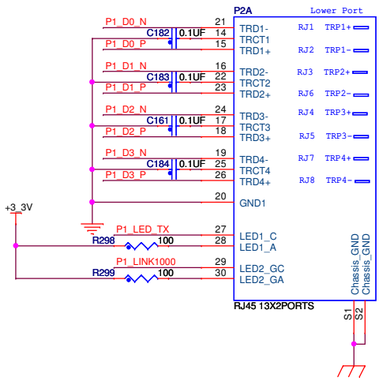


RJ45 + MAGNETICS 2X1

SGMII (eTSEC2)

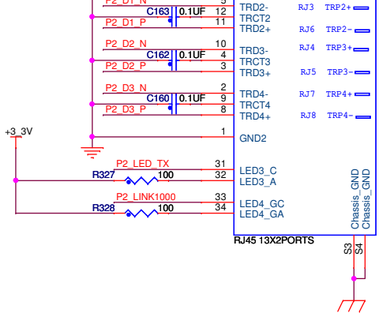


SWITCH PORT 1 & 2

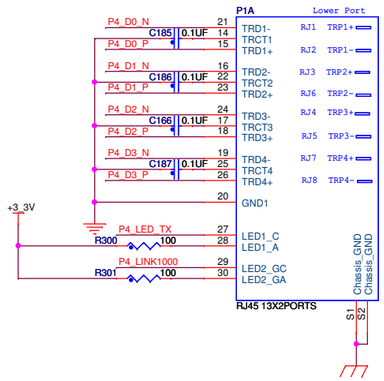


RJ45 + MAGNETICS 2X1

SGMII (eTSEC2)

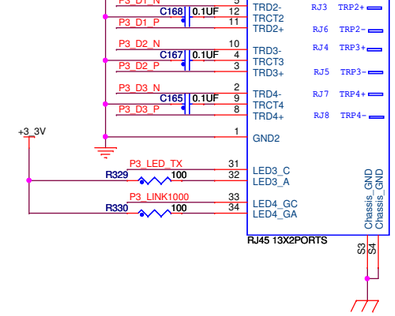


SWITCH PORT 3 & 4

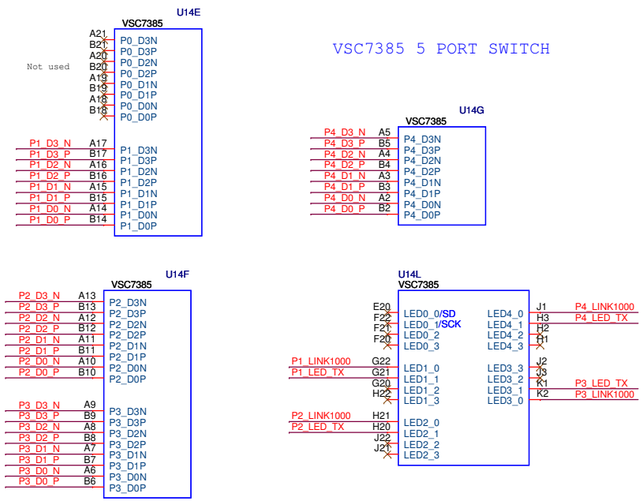


RJ45 + MAGNETICS 2X1

SGMII (eTSEC2)



VSC7385 5 PORT SWITCH



VSC7385 5 PORT SWITCH

freescale semiconductor

ICAP Classification: FCP: ___ FIUO: <FIUO> PUBI: X

Drawing Title:

RDB for P1 and P2 devices

Page Title:

Ethernet RJ-45 Ports

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POR Configuration Options

RESISTOR ONLY

RESISTOR AND PLD ACCESSIBLE

LOCAL BUS INTERFACE ADDRESS - LATCH

BUFFER

NAND FLASH

NOR FLASH

Future Expansion

These pins are SYNC_IN and SYNC_OUT on P2020 and NC for P1020.

ICAP Classification:	FCP:___ FIUO: <FIUO>PUBI: X
Drawing Title:	RDB for P1 and P2 devices
Page Title:	Local Bus and POR configs
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USB

U35 SN74LVC1G04 — VCC, NC, Y, A, GND
C330 0.1UF
DNP R412 0
USB1_FAULT_N

U40H — USB Interface (8 of 11) — P1020E
USB_D00 C26 … USB_D07 C28
USB_DIR A28, USB_STP B29, USB_NXT B26, USB_CLK D27
USB_PWRFAULT C29
USB1_FAULT
16 USB1_STP

U36 USB3300
REG_EN, VDD1_3.3, VDD3_3.3, VDD4_3.3, VDD2_3.3
VBUS_DT, DATA0–DATA7, DIR, STP, NXT, CLKOUT, RST, CPEN, VDDA1.8, GND2, GND1
DM, DP, ID, VBUS, XI, XO, RBIAS, VDD1.8, VDD1_1.8, PAD
USB1_D0 … USB1_D7, USB1_DIR, USB1_STP, USB1_NXT
USB1_CLK R156 33 USB1_CLK_S
3 RST_USB3300
USB1_CPEN
+USB1_VDDA_1_8V
C99 0.1UF, C350 4.7UF
+3_3V
C332 0.1UF, C328 0.1UF, C345 0.1UF, C346 0.1UF
USB1_D_N, USB1_D_P, USB1_ID
820 R186
USB1_XI, USB1_XO
C354 33PF, C353 33PF
Y3 24MHZ CRYSTAL
1.0M R426
USB1_RBIAS
R198 12.1K
+USB1_1_8V
C87 0.1UF, C95 4.7UF

U59 RCLAMP0504P.TCT
+USB1_PWR
L3 120OHM
L1 120OHM
C3 220UF, C1 4.7UF
DNP Host Mode R1 0

J2 USB_5_MINI_AB_SKT
USB1_VBUS, USB1_MINI_D_N, USB1_MINI_D_P, USB1_ID, USB1_GND
R27 0, R26 0
Resistors to be placed at cable header.

U1 MIC2506YM
IN, CTLA, CTLB, GND, OUTA, OUTB, FLGA, FLGB
USB1_CPEN, USB2_CPEN
+USB1_PWR, +USB2_PWR
USB1_FAULT_N, USB2_FAULT_N
R5 100K, R4 100K, R10 100K, R3 100K
C5 0.1UF
R551 DNP 1K

DNP HDR_2X5 P4
Optional cable header for front panel USB connectivity.
C517 22PF

U32 SN74LVC1G04
11 USB2_FAULT
USB2_FAULT_N
C324 0.1UF
DNP R403 0

U34 USB3300
11 USB2_D0 … USB2_D7, USB2_DIR, USB2_STP, USB2_NXT, USB2_CLK
USB2_CLK R155 33 USB2_CLK_S
3 RST_USB3300
USB2_CPEN
+USB2_VDDA_1_8V
C98 0.1UF, C348 4.7UF
C342 0.1UF, C331 0.1UF, C343 0.1UF, C327 0.1UF
USB2_D_N, USB2_D_P, USB2_ID
820 R183
USB2_XI, USB2_XO
C362 33PF, C364 33PF
Y4 24MHZ CRYSTAL
1.0M R429
USB2_RBIAS
12.1K R195
+USB2_1_8V
C86 0.1UF, C94 4.7UF

U60 RCLAMP0504P.TCT
+USB2_PWR
L4 120OHM
L2 120OHM
C4 220UF, C2 4.7UF
DNP Host Mode R2 0

J1 USB_5_MINI_AB_SKT
USB2_VBUS, USB2_MINI_D_N, USB2_MINI_D_P, USB2_ID, USB2_GND
R23 0, R24 0
Resistors to be placed at cable header.

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ICAP Classification:	FCP:___	FIUO: <FIUO>PUBI: X
Drawing Title:	RDB for P1 and P2 devices	
Page Title:	USB	
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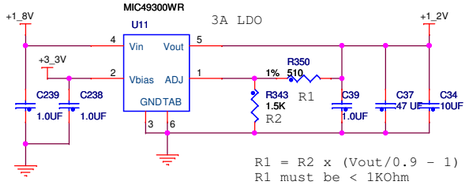
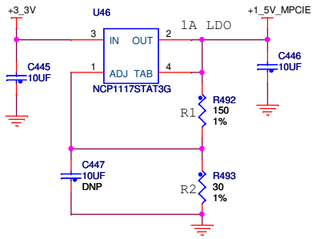
1.2V: VSC7385



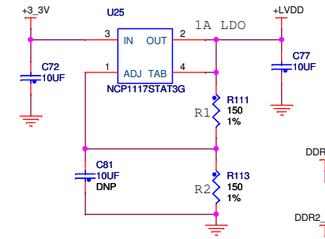
R1 = R2 x (Vout/0.9 - 1)
R1 must be < 1KOhm

1.5V: mini-PCIe connector



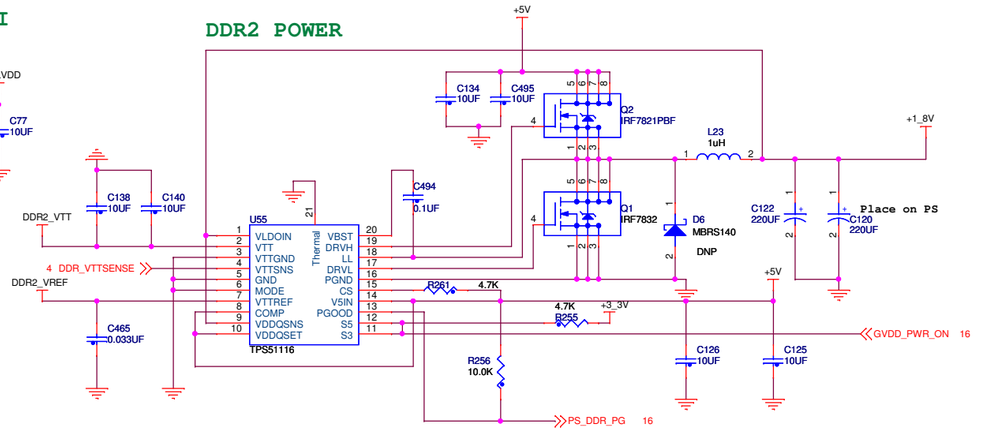
Vout=1.25x(1+R2/R1) + IadjxR2

2.5V: ETHERNET RGMII

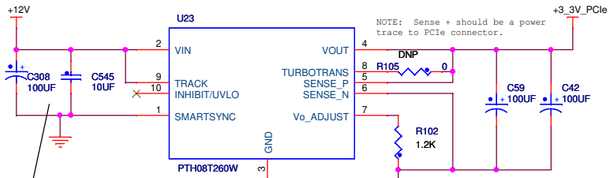


Vout=1.25x(1+R2/R1) + IadjxR2

DDR2 POWER



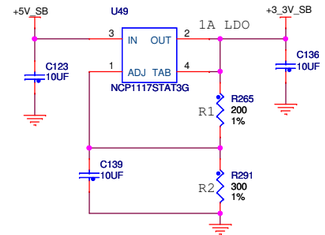
3.3V: PCIe slot



NOTE: This regulator is needed due to the limited 3.3V power from the ITX supply.

C69 is adjacent to this regulator as well.
Its a 470UF capacitor.

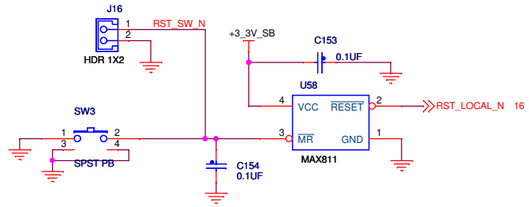
3.3V standby:



Vout=1.25x(1+R2/R1) + IadjxR2

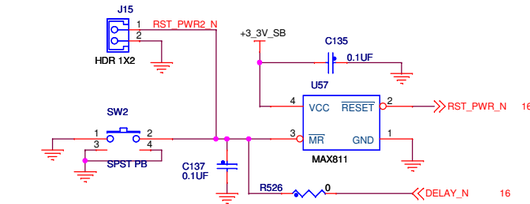
CHASSIS RESET

LOCAL RESET



CHASSIS PWR

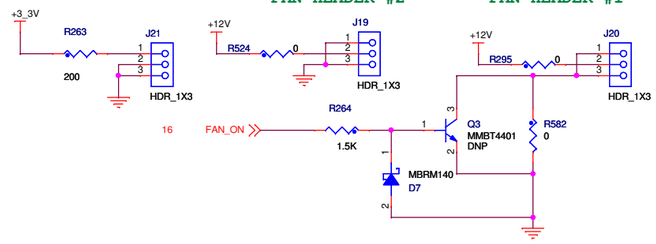
PWR SWITCH (INSIDE ITX)



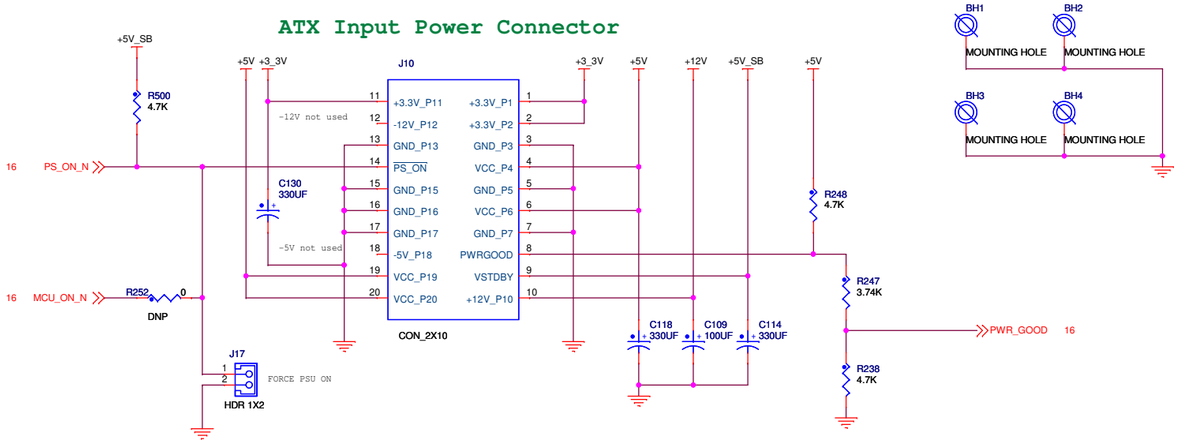
CHASSIS PWR LED

FAN HEADER #2

FAN HEADER #1



ATX Input Power Connector



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ICAP Classification: FCP: ___ FIUO: <FIUO>PUBI: X

Drawing Title: **RDB for P1 and P2 devices**

Page Title: **Misc Power & ITX Connections**

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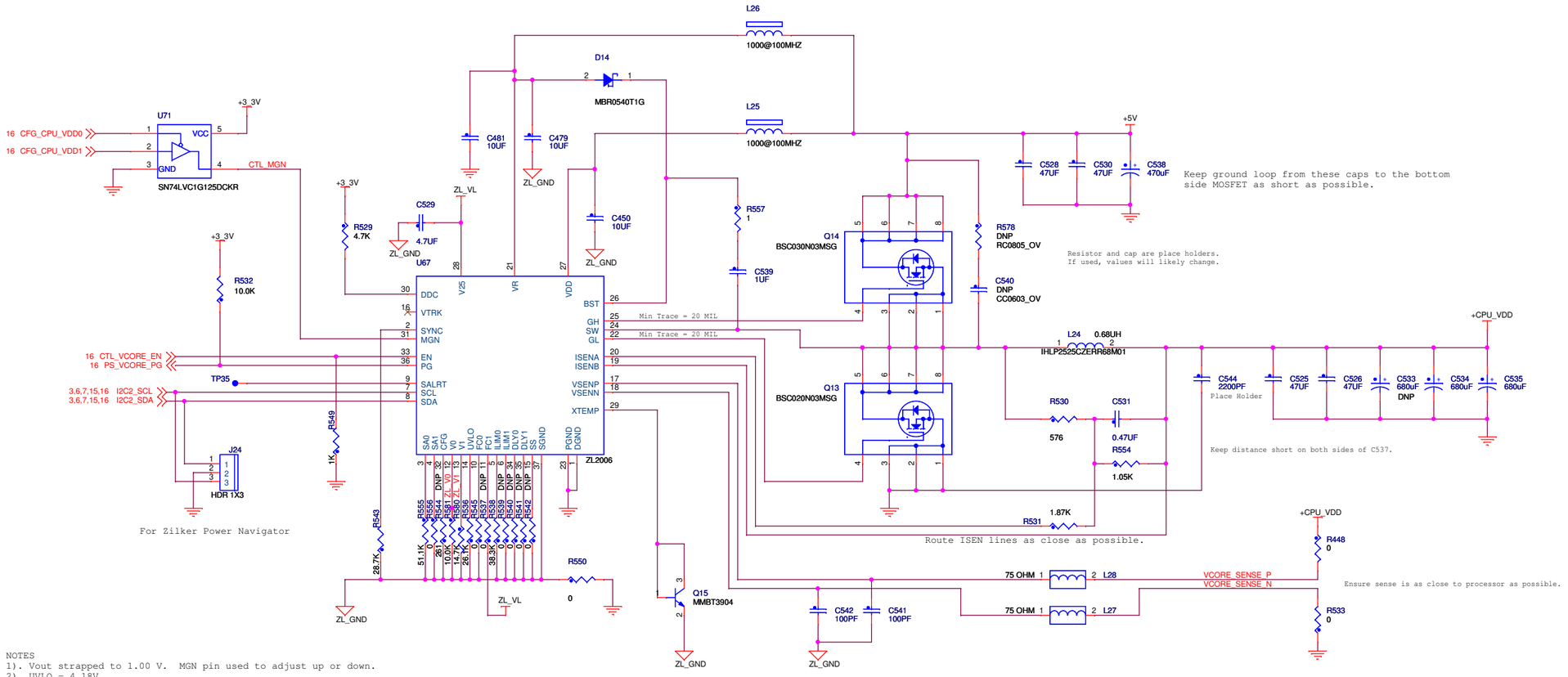
CPU VDD POWER

```
CFG_CPU_VDD[0:1] = b'01 => MGN high          VDD=1.05V    P2020 Devices
CFG_CPU_VDD[0:1] = b'00 => MGN low           VDD=0.95V    P1020 Devices
CFG_CPU_VDD[0:1] = b'1X => MGN tristated...  VDD=1.00V    P1020 Devices (second option)
```



NOTES
1). Vout strapped to 1.00 V. MGN pin used to adjust up or down.
2). UVLO = 4.18V
3). SS = 5 ms, DLY = 10 ms
4). fsw = 571kHz
5). ILIM = 70mV / 5.5mohm = 12.7A
6). I2C ADDR = 0x11
7). CFG = AUTO DETECT

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ICAP Classification: FCP:___ FIUO: <FIUO>PUBI: X

Drawing Title: **RDB for P1 and P2 devices**

Page Title: **VDD POWER SUPPLY**

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+3_3V
Y7
OSC.
VCC
EN/DIS
OUT
DGND
25MHZ
C496 0.1UF
TP27
R120
33
CLK_25M_RGMII_PHY 8

+3_3V
Y9
OSC.
C507 0.1UF
TP34
R112
33
CLK_25M_GESW 9

+3_3V
Y8
OSC.
C506 0.1UF
TP32
R114
33
CLK_25M_SGPHY1 8

NOTE: Due to weird CRCs occurring from the Ethernet PHYs, had to go with direct and separate 25MHz oscillators. Not the most efficient or cost effective, but did prove to resolve the weird CRC dilemma.

+3_3V
Y10
TRI_STATE
SUP_VOL
CASE_GND
OUTPUT
125.000MHZ
TP36
C508 0.1UF
R119
33
CLK_125M_GTX 7

+3_3V
L18
120OHM
C320 10UF
C319 0.1UF
+3_3V_ICS8304_TDMCLK

+3_3V
L17
120OHM
C322 10UF
C321 0.1UF
+3_3V_OSC_TDMCLK
X3
OSC.
2.048MHz
TP25
R129
22
TDM_CLK
U27
CLK Buffer
VDDO
VDD
CLK
GND
Q0
Q1
Q2
Q3
ICS8304AMLF
R128 33 CLK_PX020_TX_TDM 3
R121 33 CLK_RTC 3
R117 33 CLK_SLIC1_TDM 17
R116 33 CLK_SLIC2_TDM 18

TDM CLOCK

+3_3V_SB
L20
120OHM
C89 10UF
C88 0.1UF
+3_3V_OSC_SYSCLK_OPT2
X5
VDD
OE
CLK OUT
GND
100MHZ
TP26
33
R115
CLK_SYSCLK_OPT2

+3_3V_SB
L21
120OHM
C326 10UF
C325 0.1UF
+3_3V_ICSMUX_SYSCLK
U72
CLK0
CLK1
SEL0
OE
VDDO
VDD
GND
Q
clock mux
CLK_SYSCLK_66M
CLK_SYSCLK_OPT2
3,7,16 CLK_SEL
16 CLK_EN
R584 1K
R553 1K
DNP
33
R394
CLK_SYSCLK 3

+3_3V_SB
L16
120OHM
C317 10UF
C316 0.1UF
+3_3V_ICS8304_66M

+3_3V_SB
L19
120OHM
C79 10UF
C76 0.1UF
+3_3V_OSC_66M

TP24
X2
ST
VCC
GND
OUT
66.667M
33
R107
CLK_66M
U24
CLK Buffer
VDDO
VDD
CLK
GND
Q0
Q1
Q2
Q3
ICS8304AMLF
R386 33 CLK_SYSCLK_66M
R388 33 CLK_DDRCLK_66M
R390 33
R391 33
TP29
CLK_RST_PLD 16

+3_3V_SB
L22
120OHM
C503 10UF
C502 0.1UF
+3_3V_ICSMUX_DDRCLK

U73
CLK0
CLK1
SEL0
OE
VDDO
VDD
GND
Q
clock mux
CLK_DDRCLK_66M
R552 1K
16 CLK_EN
33
R397
CLK_DDRCLK 3

Only used to gate clock until power is up.

+3_3V
L15
120OHM
C71 10UF
C313 0.1UF
C310 0.1UF
C314 0.1UF
C309 0.1UF
+3_3V_ICS841_VDD

+3_3V
L11
120OHM
+3_3V_ICS841_VDDA
C303 0.1UF
C306 10UF

+3_3V
L10
120OHM
C301 10UF
C298 0.1UF
+3_3_OSC_REFCLK

U22
ICS841S04I
VDD_REF
VDD_SRC1
VDD_SRC2
VDD_SRC3
VDDA
XTAL_IN
XTAL_OUT
NC
SDATA
SCLK
IREF
VSS_REF
VSS_SRC1
VSS_SRC2
VSS_SRC3
VSSA
SRCT1_P
SRCC1
SRCT2_P
SRCC2
SRCT3_P
SRCC3
SRCT4_P
SRCC4
CLK_SD1_REFCLK_S_P 33 R101 CLK_REFCLK_P 7
CLK_SD1_REFCLK_S_N 33 R95 CLK_REFCLK_N 7
CLK_PCIE_S_P 33 R104 CLK_PCIE_P 7
CLK_PCIE_S_N 33 R103 CLK_PCIE_N 7
CLK_MPCIE_S_P 33 R108 CLK_MPCIE_P 7
CLK_MPCIE_S_N 33 R106 CLK_MPCIE_N 7
R381 51
R380 51
R384 51
R383 51
R389 51
R387 51
ICS841_IREF
R378 475 1%

X1
OSC.
VCC
EN/DIS
OUT
DGND
25MHZ
TP21
R86 33
CLK_ICS841_25MHZ
3,6,7,14,16 I2C2_SDA
3,6,7,14,16 I2C2_SCL

I2C2 ADDRESS => 69H

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ICAP Classification: FCP:___ FIUO: <FIUO>PUBI: X

Drawing Title: **RDB for P1 and P2 devices**

Page Title: **Clocking**

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NOR FLASH BANK SELECTION

REV B and later - uses new switch option. See SW4
REV A - uses two pin option denoted below

When Jumper is across pins 7-8, low bank selected.
When Jumper is across pins 7-9, high bank selected.

Switch2 - Used to be called cpu_sel on Rev A board.

CPU_SEL = 0 (P2020)
CPU_SEL = 1 (P1020)

SW4 — 218-8LPST

U37 — EPM7064AETC44-10N

SWITCH2 37 — IN/GCLK1
CFG_DRV_N 38 — IN/OE1
SWITCH1 39 — IN/GCLRN
SWITCH3 40 — IN/OE2/GCLK2

PLD1_TDO 1 — I/O1/TDI
PLD_TMS 7 — I/O7/TMS
PLD_TCK 26 — I/O26/TCK
PLD2_TDO 32 — I/O32/TDO

SWITCH4 2 — I/O2
SWITCH5 3 — I/O3
SWITCH6 5 — I/O5
6 — I/O6
8 — I/O8
10 — I/O10
11 — I/O11
12 — I/O12
13 — I/O13
14 — I/O14
15 — I/O15

36 — GNDINT
16 — GNDINT
24 — GNDIO
4 — GNDIO

VCCIO 9, 29
VCCIO 17
VCCINT 39
VCCINT 41

I/O44 — LRCTL 11, LALE2
I/O43 — LGPL2 11
I/O42 — LA24 9,11
I/O35 — LA27 9,11
I/O34 — LWE0_N 11
I/O33
I/O31 — PLD_UART1_SOUT 7
I/O30 — READY_P1 3,11
I/O28 — LA25 9,11
I/O27 — LA16 9,11
I/O25 — LA29 9,11
I/O23 — LA30 9,11
I/O22 — LA31 9,11
I/O21 — BOOT_SEL 11
I/O20 — LA23 9,11
I/O19 — LA26 9,11
I/O18 — DMA1_DDONE_N 3,11

FBANK_SELECT
7 PLD_1588_CLK_OUT
7 PLD_1588_PULSE_OUT1
7 PLD_1588_PULSE_OUT2
7 PLD_TSEC3_TXD2
7 PLD_TSEC3_TXD1
7 PLD_TSEC3_TXD0
7 PLD_TSEC1_TX_ER
3,11 MSRCID0

LGPL5 — LGPL5 16 — cfg_boot_seq[1]

NOTE: NON-STANDARD connection on pins 6, 7, and 8 of P7.

P7 — HDR_2X5
R528 0
R574 0
R525 1K
R521 1K
R522 1K
R515 0
R520 DNP
R516 1K
R519 0
PLD_TMS
PLD_TCK
PLD1_TDO
PLD2_TDO
SWITCH2

Input pins are 5V tolerant.

U56 — EPM7064AETC44-10N

15 CLK_RST_PLD
RST_LCL_N
RST_PLD_N
3 HRSTREQ_N
PLD_TDI

3,7,15 CLK_SEL
6 COP_HRST_N
6 COP_TRST_N
6 COP_SRST_N
13 PS_ON_N
14 CTL_VCORE_EN
14 PS_VCORE_PG
13 PWR_GOOD
3,7 ALERT_N
13 PS_DDR_PG

CPU_SRST_N 3
CPU_TRST_N 3
CFG_DRV_N
CLK_EN 15
THERM_FAULT
CFG_DRV2_N 7
RST_PWR_N 13
CPU_HRST_N 3
DELAY_N 13
FBANK_SELECT
GVDD_PWR_ON 13
FBANK_SEL 11
RST_FLSH_N 11

Switch2 - Used to be called cpu_sel on Rev A board.

CLK_SEL - Used to be called gpi10 on Rev A board.

HDR_1X3 J12
R583 300
D15 LED RED

CFG_CPU_VDD[0:1] = b'1X gives 1.00V
CFG_CPU_VDD[0:1] = b'01 gives 1.05V
CFG_CPU_VDD[0:1] = b'00 gives 0.95V

SW5 — 218-8LPST

CFG_CPU_VDD0 14
CFG_CPU_VDD1 14
TEST_SEL 3
DMA1_DACK_N 3
SW_USB1_STP
CFG_SDWIDTH 6
CLK_SEL 3,7,15
LA19 11 — cfg_host_agt[2]
LWE1_N 11 — cfg_host_agt[0]

J25 — HDR 1X2

P2020/P1020
-- TEST_SEL = 1
-- DMA_DACK = 1
-- USB1_STP = 1

CFG_DRV2_N
R535 1K

U76 — SN74LVC1G125DCKR
USB1_STP 12

U77 — SN74LVC1G125DCKR
11 LALE2 — LALE 11

Used to minimize length on LALE

U78 — SN74LVC1G125DCKR
3 HRST_REQ_N — HRSTREQ_N 12

C497 0.1UF
U66 — MAX811
RST_PLD_N

C504 0.1UF
U74 — PCA9557PW
R575 1K DNP
TP31 Open drain output

CFG_SDWIDTH
FBANK_SELECT
SWITCH6
SWITCH5
SWITCH4
SWITCH3
SWITCH2
SWITCH1

Can be read and written by software.

3,6,7,14,15 I2C2_SCL
3,6,7,14,15 I2C2_SDA

RESET — Resets during power cycle.

I2C2 ADDRESS:
"0011,A2,A1,A0" = 18H

Micro-controller shown below not currently used.

HDR_1X8 J18
R293 300
R294 300
LED2_K
LED1_K

D12 MBRM140
D11 MBRM140
VBAT_OPT2 6

IDD max 120mA @ 3.3V = .396W

D8 LED_GRN_DL
D9 LED_GRN_DL
LED2_A
LED1_A
C448 22UF
C449 0.1UF

U64 — MC9S08QG8

PTA0/KBIP0/TPMCH0/ADP0/ACMP+
PTA1/KBIP1/ADP1/ACMP-
PTA2/KBIP2/SDA/ADP2
PTA3/KBIP3/SCL/ADP3
PTA4/ACMPO/BKGD/MS
PTA5/IRQ/TCLK/RESET
PTB0/KBIP4/RxD/ADP4
PTB1/KBIP5/TxD/ADP5
PTB2/KBIP6/SPSCK/ADP6
PTB3/KBIP7/MOSI/ADP7
PTB4/MISO
PTB5/TPMCH1/SS
PTB6/SDA/XTAL
PTB7/SCL/EXTAL
VDD
VSS

13 PWR_GOOD — R251 0 DNP
3,6 I2C1_SDA
3,6 I2C1_SCL
13 RST_PWR_N
LED2_K
R249 0
R246 0
R253 4.7K DNP
R423 4.7K
FAN_ON 13
MCU_INT_N 3
LED1_K

J14 — HDR 2X3
MCU DEBUG HEADER

R494 10M
Y6 32.768KHZ
C443 22PF
C444 22PF

MCU I2C ADDR => 0AH

J13 — HDR 1X2
Boot loader jumper.
ON - MCU boots up in boot loader mode.
OFF - Normal operation.

R250 0 DNP
13 RST_LOCAL_N — R254 0 — RST_LCL_N

MCU_ON
R498 1K
Q7 MMBT4401
MCU_ON_N 13

J7 — HDR_2X4
3,7,11 UART1_SOUT
6 UART1_SOUT_OUT
UART1_SIN 3
UART1_SIN_OUT 6
R579 4.7K

Pull-down added so that jumper is not needed by default. Only when UART1 is needed are jumpers required.

1-3; 2-4 : CPU UART2 CONNECTED TO DB9 (DEFAULT)
3-5; 4-6: MCU CONNECTED TO DB9
5-7; 6-8: MCU CONNECTED TO CPU

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ICAP Classification: FCP:___ FIUO: PUBI: X

Drawing Title: RDB for P1 and P2 devices

Page Title: Reset, RCW PLDs, Optional MCU

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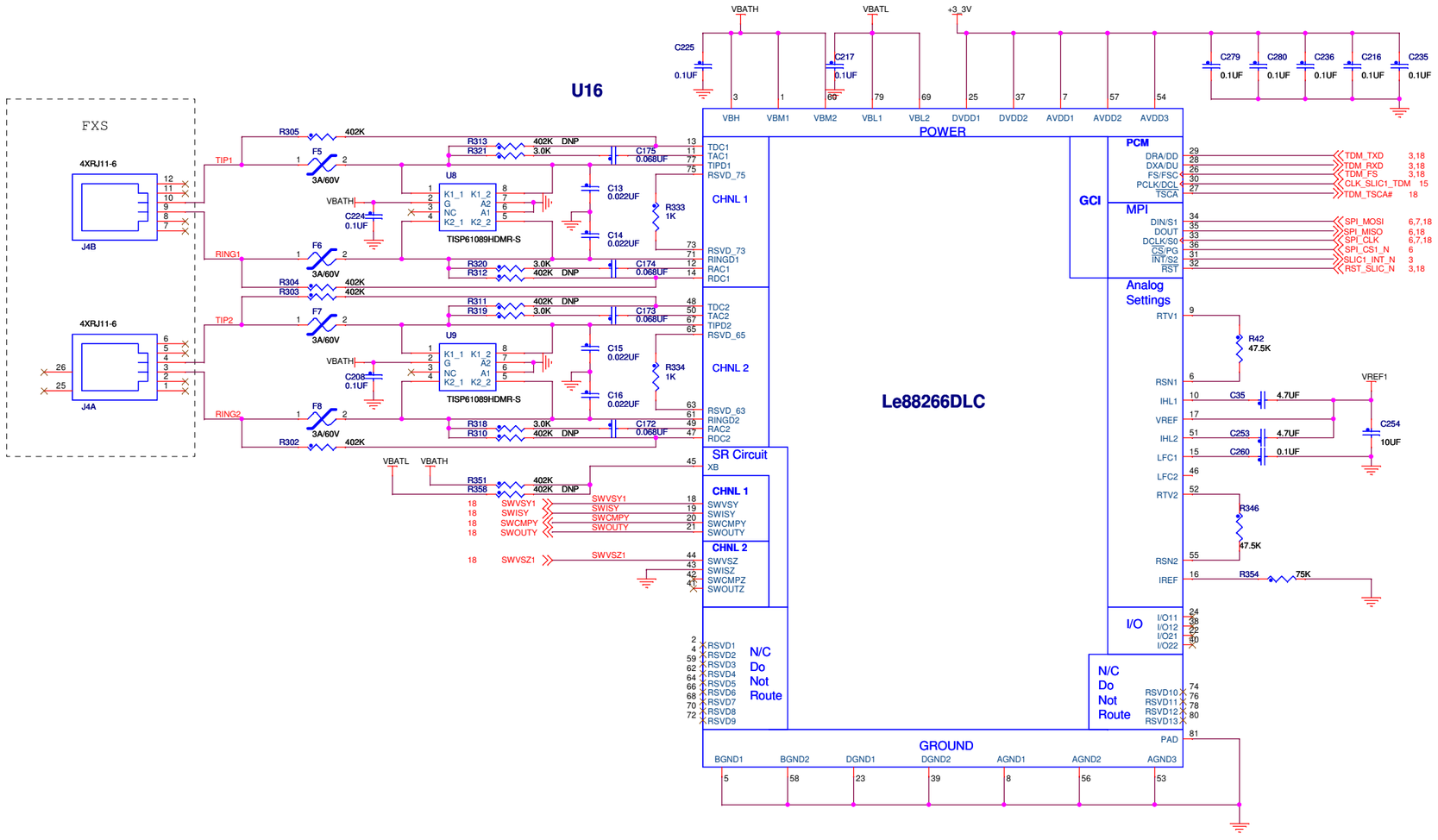
SLIC INTERFACE_1

VOICE PORT 1 & 2



This sheet is only applicable for devices that have a TDM Port. For example, P1020.
TDM Port not Available for P2020

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ICAP Classification:	FCP: ___ FIUO:	PUBI: X
Drawing Title:	**RDB for P1 and P2 devices**	
Page Title:	**SLIC INTERFACE 1**	
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SLIC INTERFACE_2

VOICE PORT 3 & 4

U15

Le88266DLC

POWER: VBH, VBM1, VBM2, VBL1, VBL2, DVDD1, DVDD2, AVDD1, AVDD2, AVDD3

GROUND: BGND1, BGND2, DGND1, DGND2, AGND1, AGND2, AGND3, PAD

CHNL 1 / CHNL 2

SR Circuit: XB; CHNL 1: SWVSY, SWISY, SWCMPY, SWOUTY; CHNL 2: SWVSZ, SWISZ, SWCMPZ, SWOUTZ

GCI

PCM: DRA/DD, DXA/DU, FS/FSC, PCLK/DCL, TSCA

MPI: DIN/S1, DOUT, DCLK/S0, CS/PG, INT/S2, RST

Analog Settings: RTV1, RSN1, IHL1, VREF, IHL2, LFC1, LFC2, RTV2, RSN2, IREF

I/O: I/O11, I/O12, I/O21, I/O22

N/C Do Not Route: RSVD1–RSVD9

N/C Do Not Route: RSVD10–RSVD13

FXS

4XRJ11-6 J4D, J4C

TISP61089HDMR-S U6, U7

F1–F4 3A/60V

AGN200A03 K1

D1 1N4148WS

FXO

J5 HDR 1X2

NOTE:
Connected
to Panel
mount RJ11

RELAY STATE

STATE	TIP_FXS Connected to	RING_FXS Connected to
ENERGIZED	TIP4 (FXS)	RING4 (FXS)
DEENERGIZED	TIP_FXO	RING_FXO

This sheet is only applicable for devices that have a TDM Port. For example, P1020.
TDM Port not Available for P2020

SLIC POWER SUPPLY

The red color line indicates high current path. Short and wide traces should be used with minimal vias.

T1 C8140

D3 MURS120T3

D5 MURS120T3

D4 BAW56-7-F

D2 ES1D-13-F

Q5 MMBT2907A

Q4 FQD30N06LTF

Q6 FDV301N

Place near SLIC

DNP: C44 4.7PF; C45 4700 PF; R66 402K; C546 330PF

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ICAP Classification: FCP: ___ FIUO: PUBI: X

Drawing Title: RDB for P1 and P2 devices

Page Title: SLIC INTERFACE 2

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