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Revisions

C	Release for PCB Rev C to support P1020E.	May 2009	Austin HW
D	Fixed all outstanding errata (CE5 - CE16)	Jan 2010	Austin HW

RDB supporting P1020, P1011, P2020, P2010 Devices

Schematic is used for different P1 and P2 devices.
The DNPs shown in this schematic accommodate P1020.

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NMG
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: FCP: ____ FIUO: PUBI: X

Designer: Austin HW	Drawing Title: **RDB for P1 and P2 Devices**		
Drawn by: Austin HW	Page Title: **Cover and TOC**		
Approved: Austin HW	Size C	Document Number SCH-26158 PDF: SPF-26158	Rev D
	Date: Monday, February 01, 2010	Sheet 1 of 18	

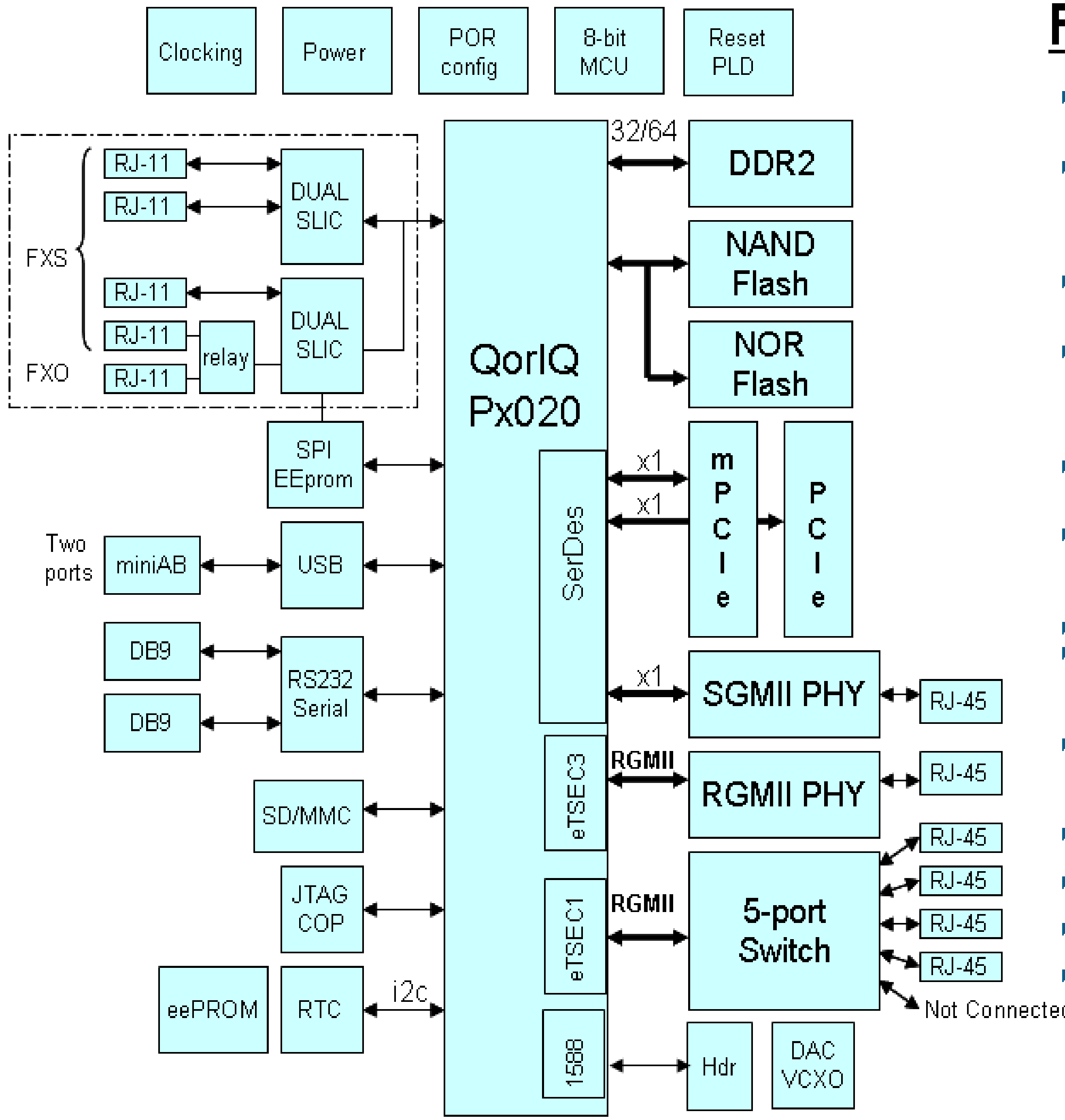
1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/8 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.



RDB Platform

- Common PCB supporting
  - P1020 @ 800 MHz core speed 0.95V
  - P2020 @ 1.2 GHz core speed 1.05V
- Memory
  - DDR2 – 512MB/1GB/2GB
  - NOR Flash – 16Mbyte (128Mbit device)
  - NAND Flash – 32MByte
  - SPI ROM – 16MByte
- PCIe
  - One standard PCIe connector (x1)
  - One mini PCIe connector (x1)
- Ethernet
  - Six 10/100/1000 ports as follows:
  - 4-ports from L2 switch connected to eTSEC1
  - 1 SGMII PHY connected to eTSEC2
  - 1 RGMII PHY connected to eTSEC3
- 1588
  - Clock input from DAC / VCXO circuitry
  - Accessible via test header
- I2C
  - Serial eePROM – boot loader
  - Serial eePROM – board identification
  - RTC
- SD/MMC card slot
- TDM
  - Support Legerity Dual SLIC
  - 4 FXS ports
  - 1 FXO port via relay
- USB
  - Option #1 -Two Mini AB connectors on IO Panel (default)
  - Option #2 –Two Type A connectors (front panel)
- MCU
  - 8-bit FSL microcontroller
- UARTs
  - Two DB9 connectors
- Form Factor
  - Mini-ITX chassis
- Schematics – OrCad; PCB - Allegro

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ICAP Classification:	FCP: ___	FIUO:	PUBI: _x_
Drawing Title:	RDB for P1 and P2 devices		
Page Title:	Block Diagram		
Size C	Document Number SCH-26158 PDF: SPF-26158		Rev D
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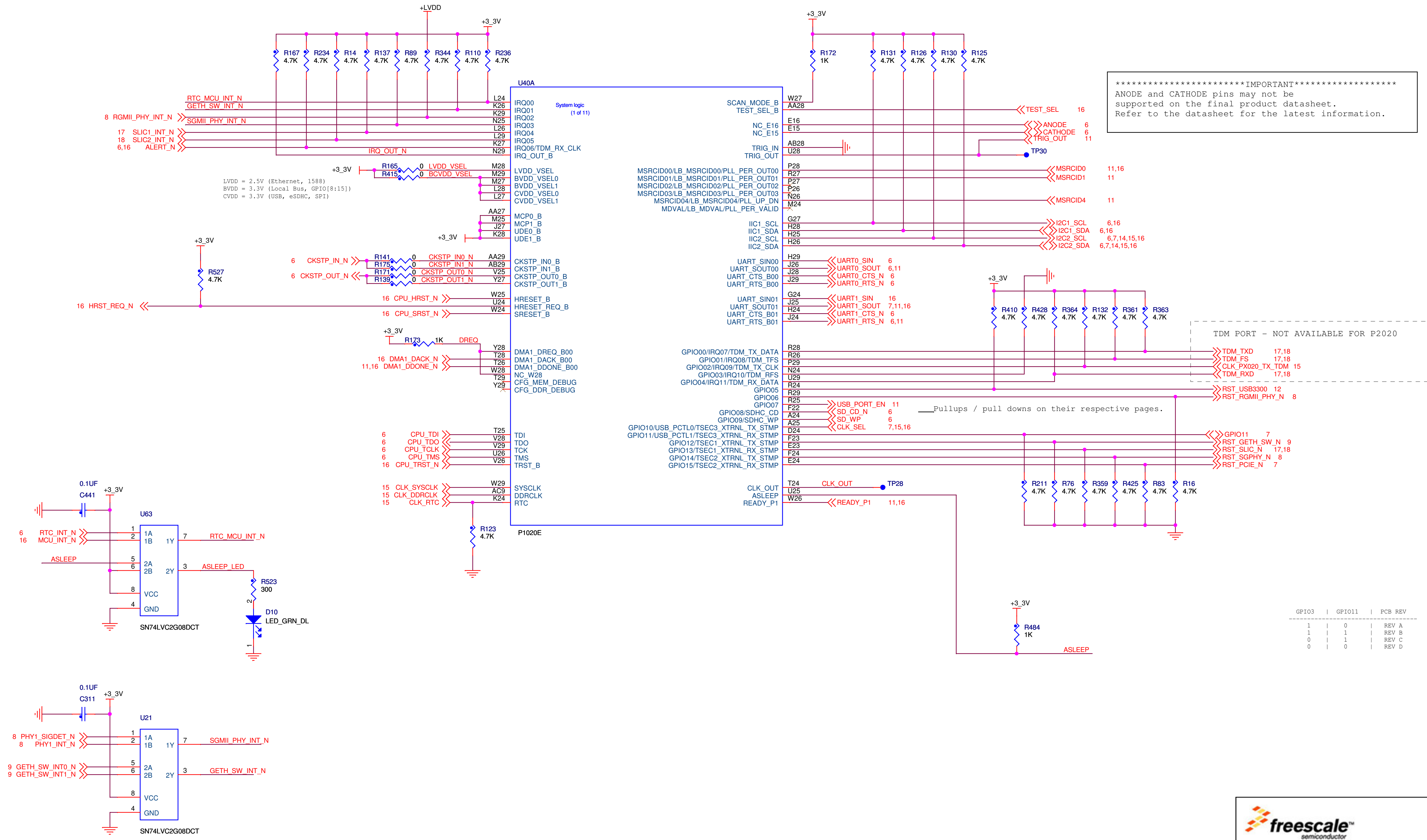

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ICAP Classification: FCP: ___ FIUO: <FIUO>PUBI: X

Drawing Title: **RDB for P1 and P2 devices**

Page Title: **CPU Misc**

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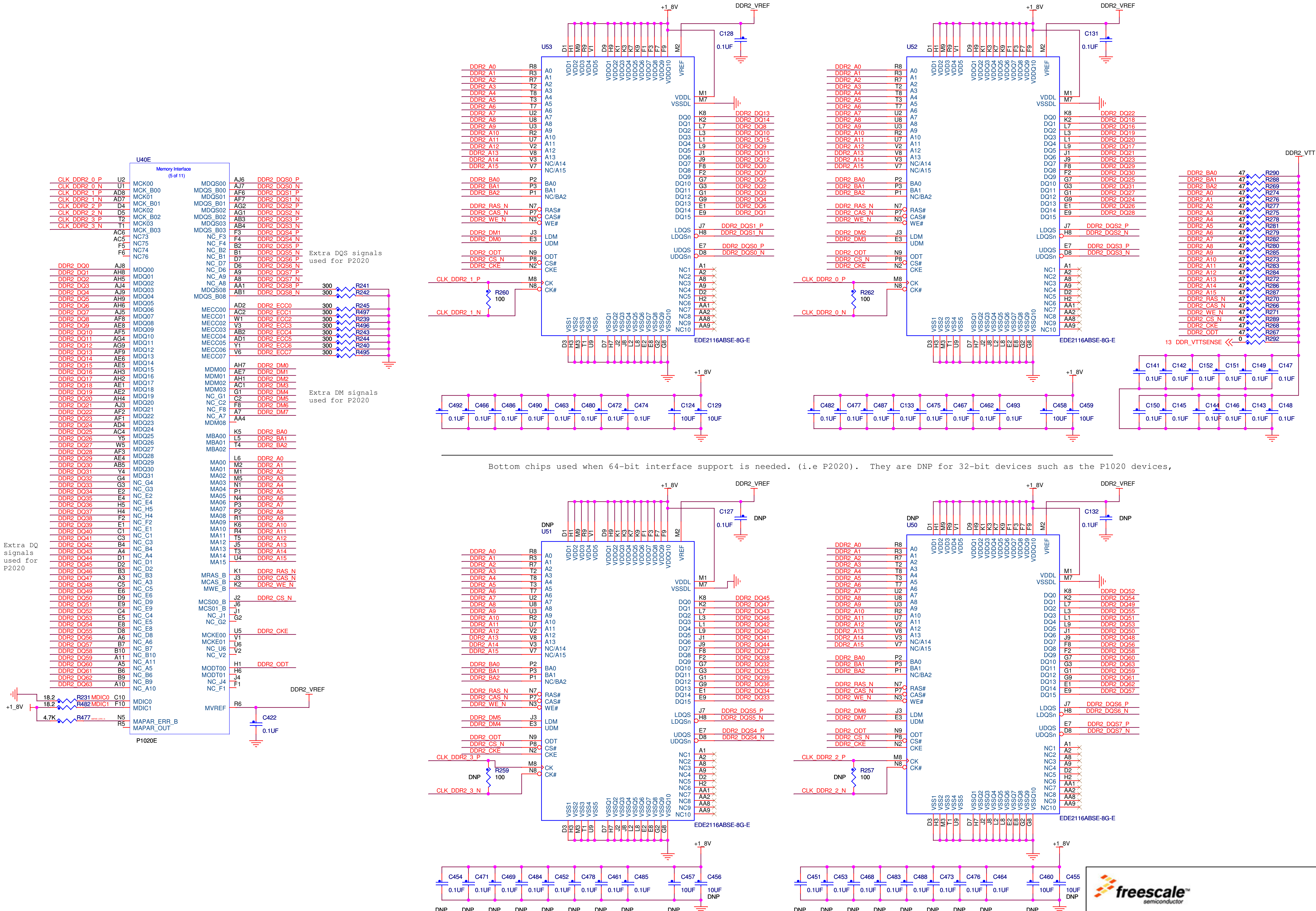

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ICAP Classification: FCP: ___ FIUO: <FIUO>PUBI: X

Drawing Title:
RDB for P1 and P2 devices

Page Title:
DDR2 Memory

Size	Document Number	Rev
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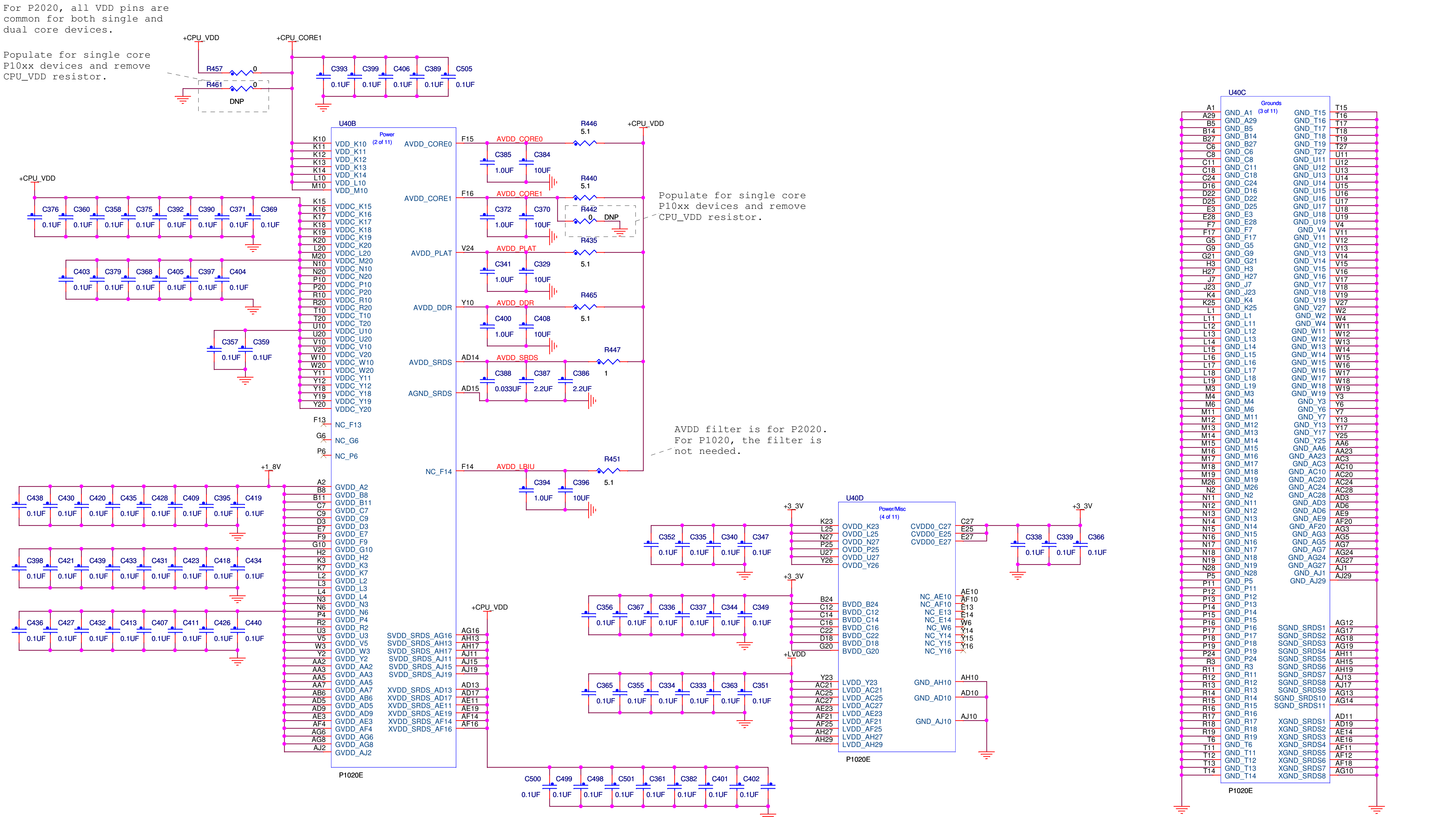

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ICAP Classification:	FCP: ___	FIUO: <FIUO> PUBI: X
Drawing Title:	RDB for P1 and P2 devices	
Page Title:	CPU Power and Ground	
Size C	Document Number SCH-26158 PDF: SPF-26158	Rev D
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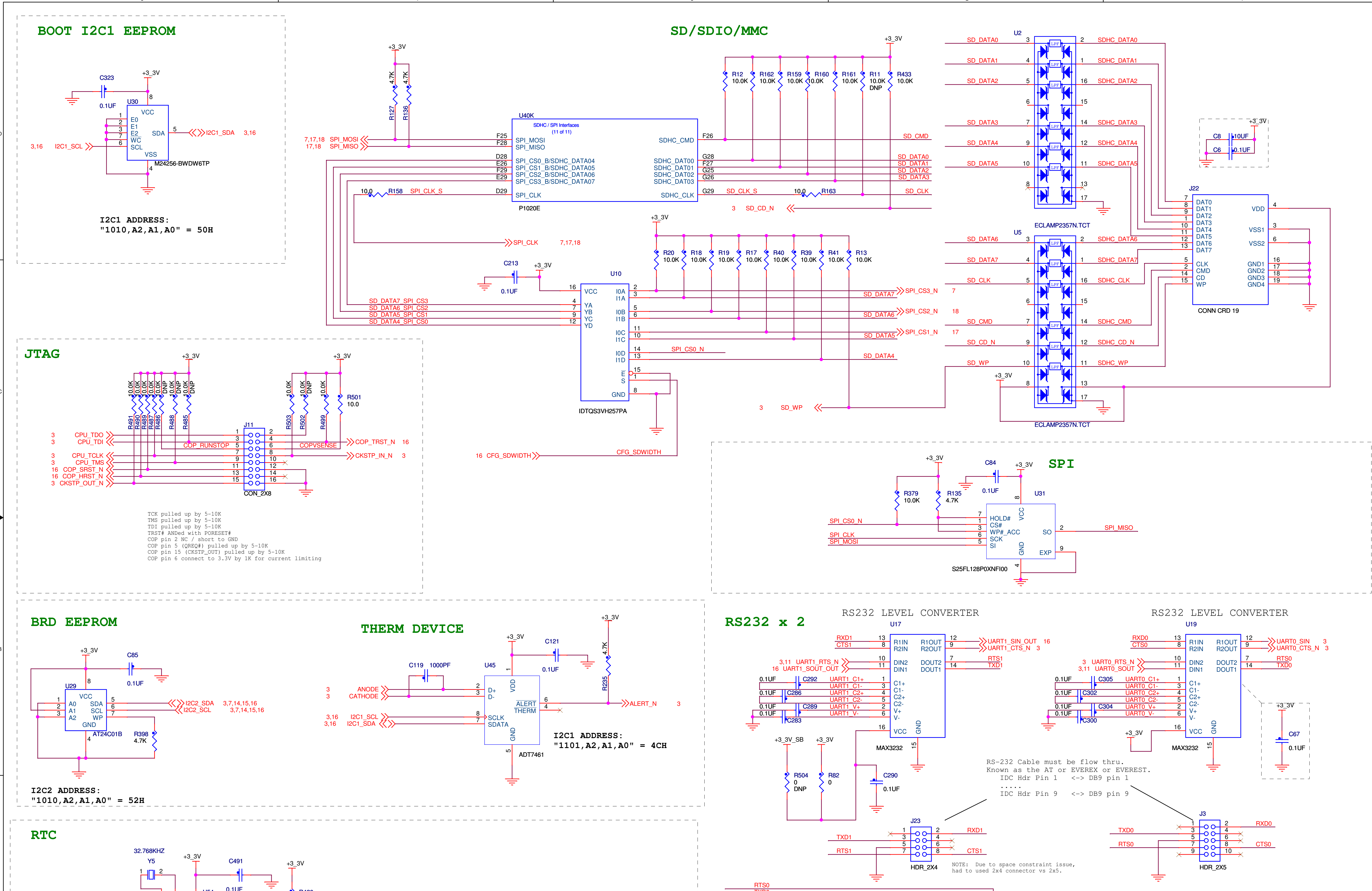

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ICAP Classification: FCP: ___ FIUO: <FIUO>PUBI: X

Drawing Title: **RDB for P1 and P2 devices**

Page Title: **I2C, SPI, SD/MMC, JTAG, RS232, RTC**

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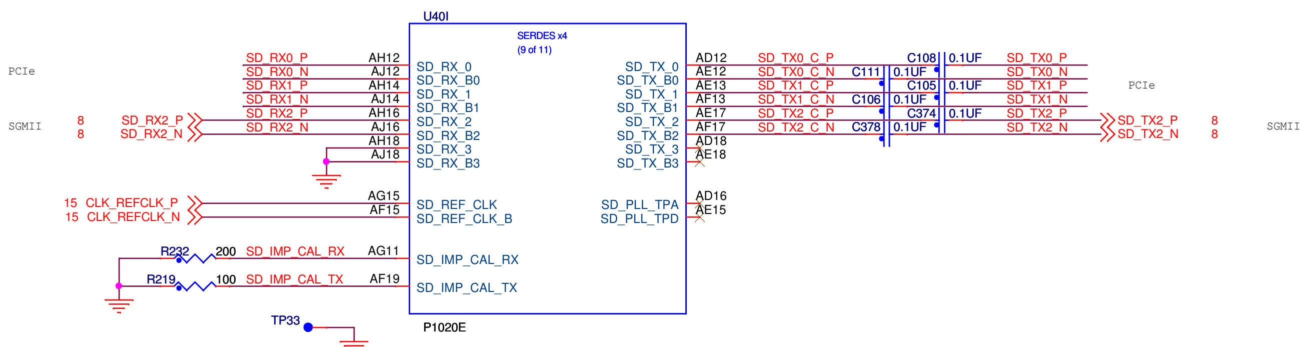
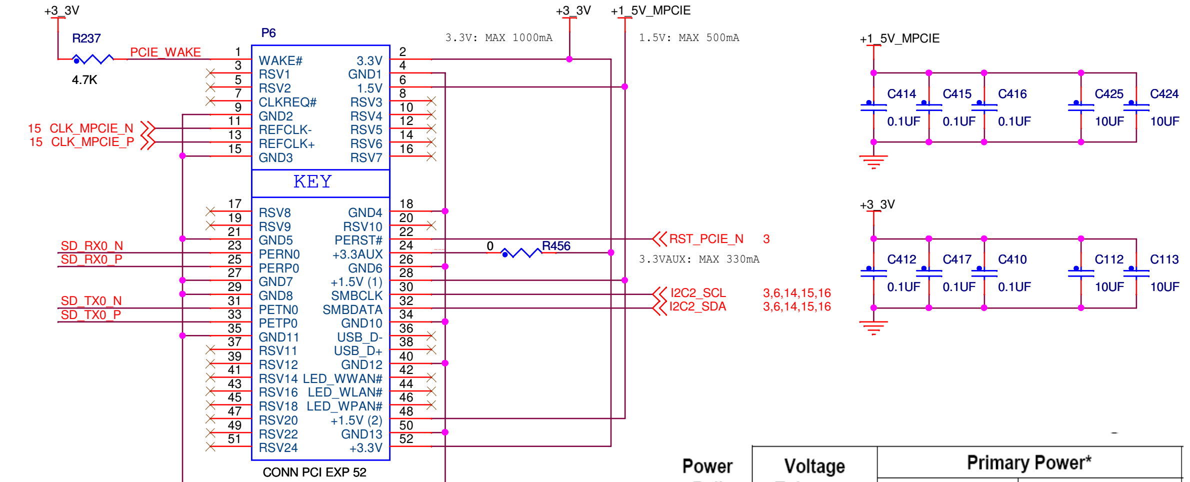


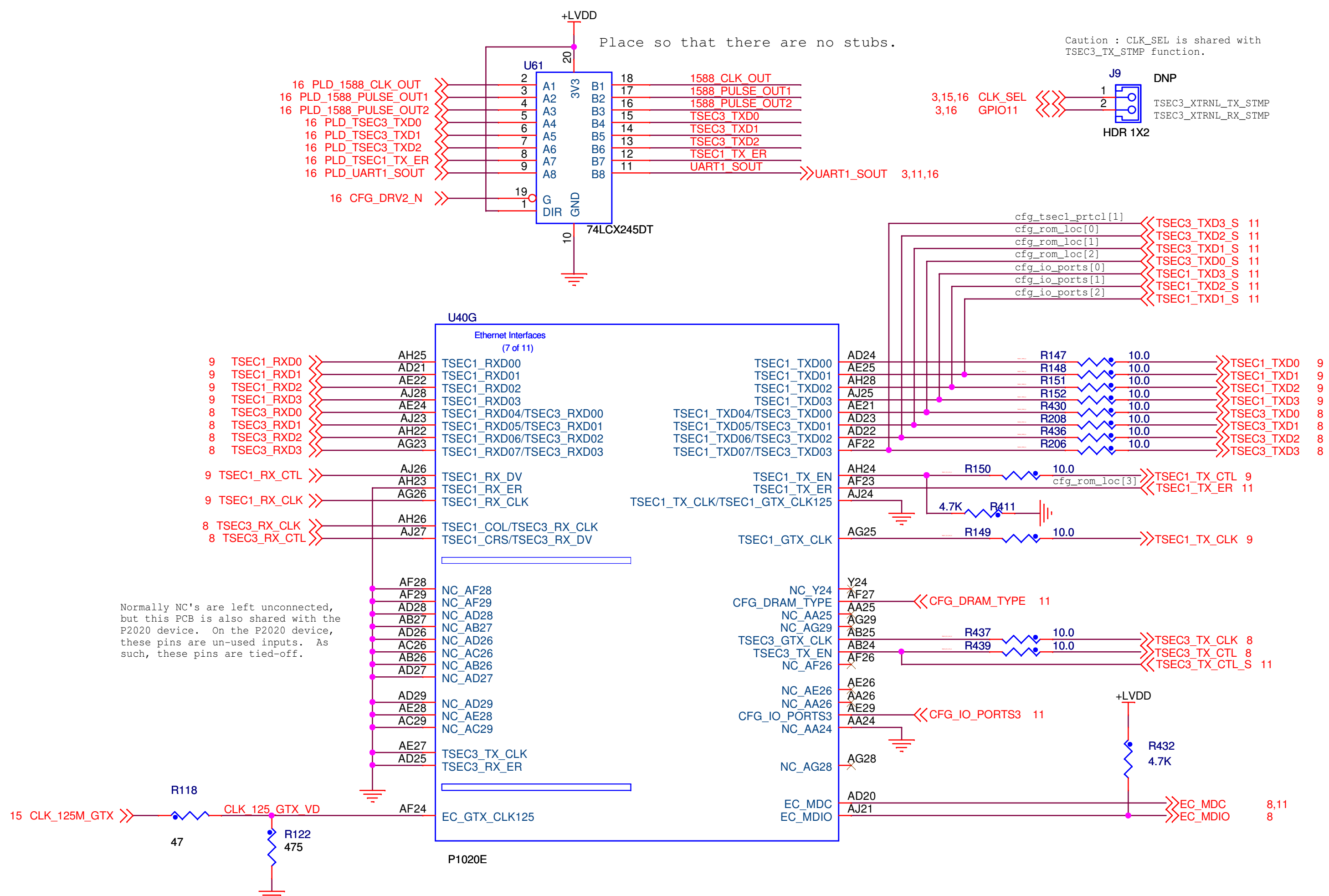


Mini PCI Express Connector

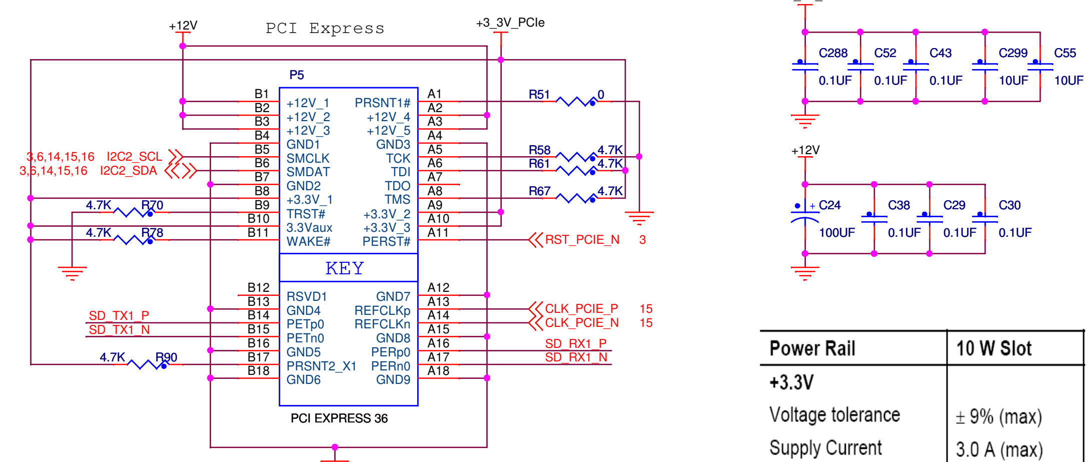
Power Rail	Voltage Tolerance	Primary Power*	
		Peak (max) mA	Normal (max) mA
+3.3V	±9%	1,000	750
3.3Vaux	±9%	330	250
+1.5V	±5%	500	375

Place so that there are no stubs.

Caution : CLK_SEL is shared with TSEC3_TX_STMP function.



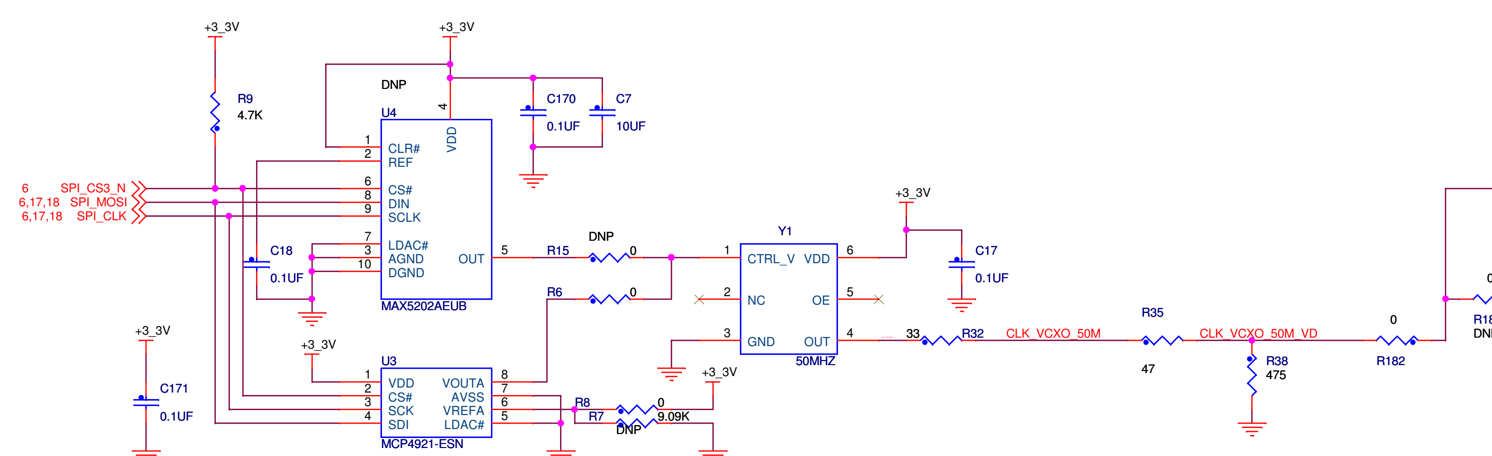
PCI Express

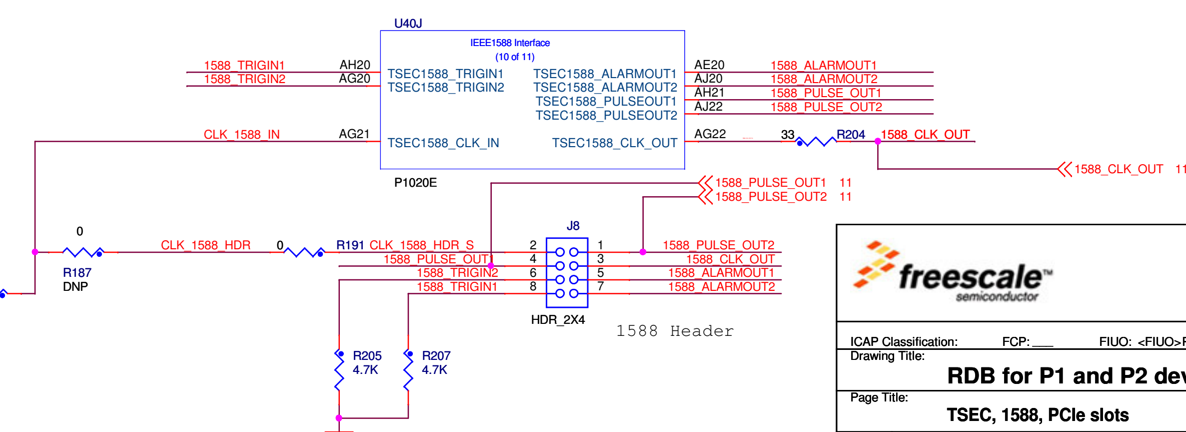


IMPORTANT - x1 PCIe cards are rated as 10W are less.
As such, only x1 PCIe cards are allowed in this slot.
Secondly, the chassis supply can only support x1 PCIe cards.

Power Rail	10 W Slot
+3.3V	
Voltage tolerance	± 9% (max)
Supply Current	3.0 A (max)
Capacitive Load	1000 μF (max)
+12V	
Voltage tolerance	± 8%
Supply Current	0.5 A (max)
Capacitive Load	300 μF (max)

NOTE: 1588 Interface Powered off LVDD = 2.5V





1588 Header

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ICAP Classification: FCP:___ FIUO: <FIUO>PUBI: X

Drawing Title: **RDB for P1 and P2 devices**

Page Title: **TSEC, 1588, PCIe slots**

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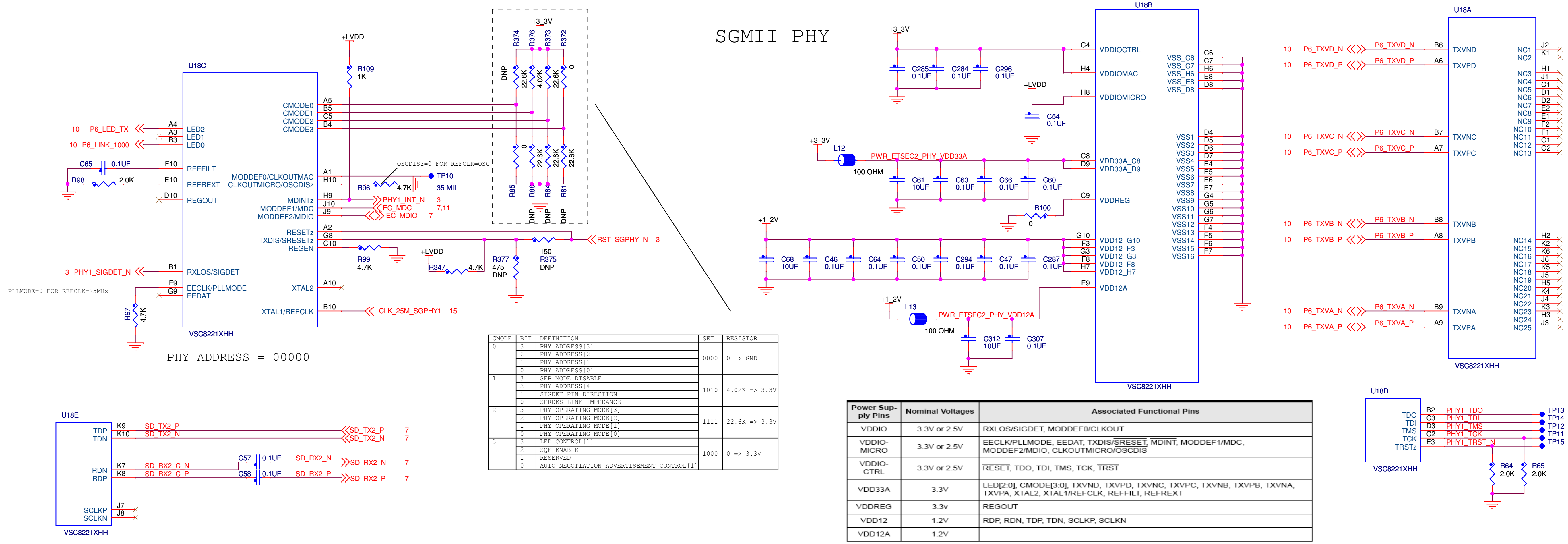
SGMII PHY



PHY ADDRESS = 00000

CMODE	BIT	DEFINITION	SET	RESISTOR
0	3	PHY ADDRESS[3]	0000	0 => GND
	2	PHY ADDRESS[2]		
	1	PHY ADDRESS[1]		
	0	PHY ADDRESS[0]		
1	3	SFP MODE DISABLE	1010	4.02K => 3.3V
	2	PHY ADDRESS[4]		
	1	SIGDET PIN DIRECTION		
	0	SERDES LINE IMPEDANCE		
2	3	PHY OPERATING MODE[3]	1111	22.6K => 3.3V
	2	PHY OPERATING MODE[2]		
	1	PHY OPERATING MODE[1]		
	0	PHY OPERATING MODE[0]		
3	3	LED CONTROL[1]	1000	0 => 3.3V
	2	SQE ENABLE		
	1	RESERVED		
	0	AUTO-NEGOTIATION ADVERTISEMENT CONTROL[1]		

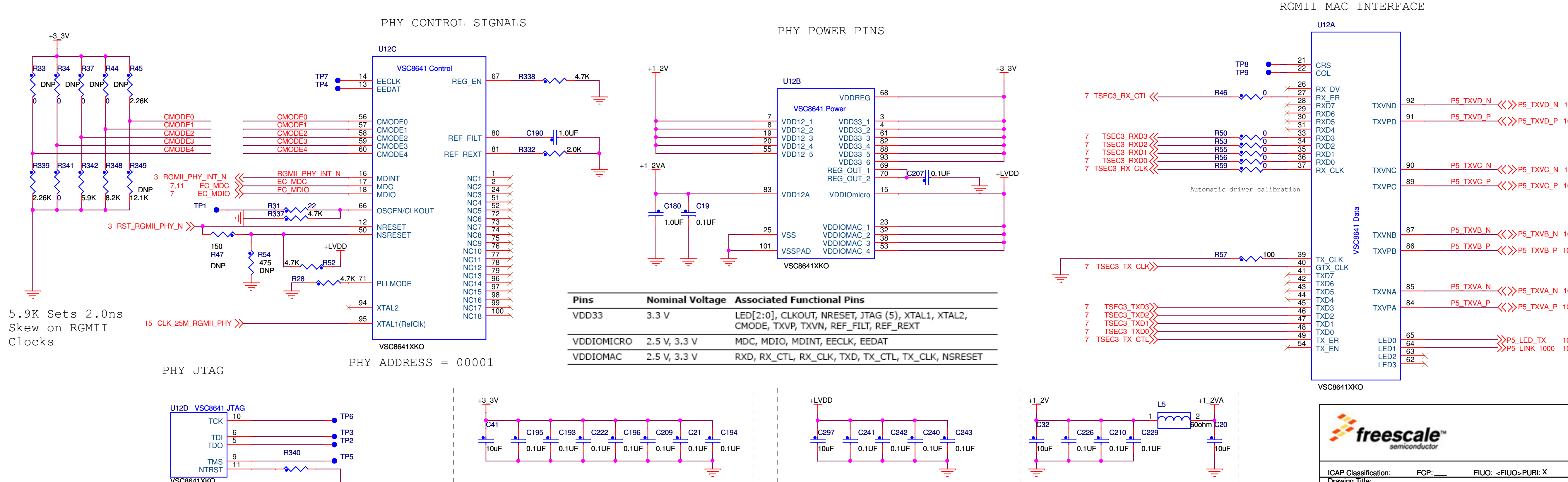
Power Supply Pins	Nominal Voltages	Associated Functional Pins
VDDIO	3.3V or 2.5V	RXLOS/SIGDET, MODDEF0/CLKOUT
VDDIO-MICRO	3.3V or 2.5V	EECLK/PLLMODE, EEDAT, TXDIS/SRESET, MDINT, MODDEF1/MDC, MODDEF2/MDIO, CLKOUTMICRO/OSCDIS
VDDIO-CTRL	3.3V or 2.5V	RESET, TDO, TDI, TMS, TCK, TRST
VDD33A	3.3V	LED[2:0], CMODE[3:0], TXVND, TXVPD, TXVNC, TXVPC, TXVNB, TXVPB, TXVNA, TXVPA, XTAL2, XTAL1/REFCLK, REFFILT, REFREXT
VDDREG	3.3v	REGOUT
VDD12	1.2V	RDP, RDN, TDP, TDN, SCLKP, SCLKN
VDD12A	1.2V	

RGMII PHY

PHY CONTROL SIGNALS

PHY POWER PINS

RGMII MAC INTERFACE



5.9K Sets 2.0ns Skew on RGMII Clocks

PHY JTAG

PHY ADDRESS = 00001

Pins	Nominal Voltage	Associated Functional Pins
VDD33	3.3 V	LED[2:0], CLKOUT, NRESET, JTAG (5), XTAL1, XTAL2, CMODE, TXVP, TXVN, REF_FILT, REF_REXT
VDDIOMICRO	2.5 V, 3.3 V	MDC, MDIO, MDINT, EECLK, EEDAT
VDDIOMAC	2.5 V, 3.3 V	RXD, RX_CTL, RX_CLK, TXD, TX_CTL, TX_CLK, NSRESET

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ICAP Classification: FCP: ___ FIUO: <FIUO>PUBI: X

Drawing Title: **RDB for P1 and P2 devices**

Page Title: **Ethernet Phys**

Size	Document Number	Rev
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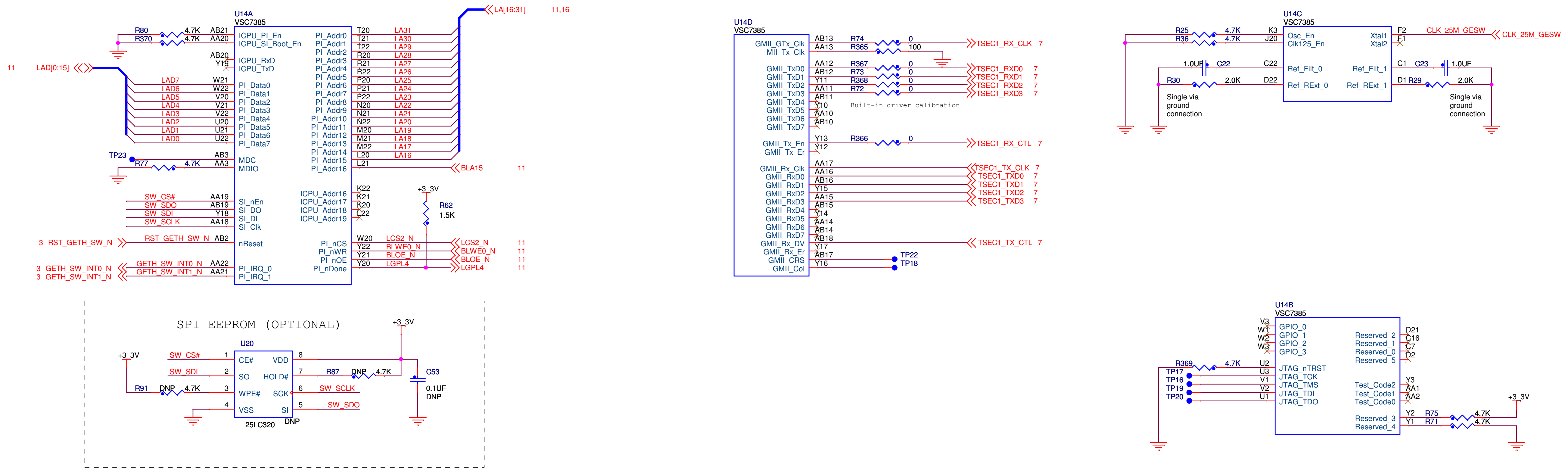
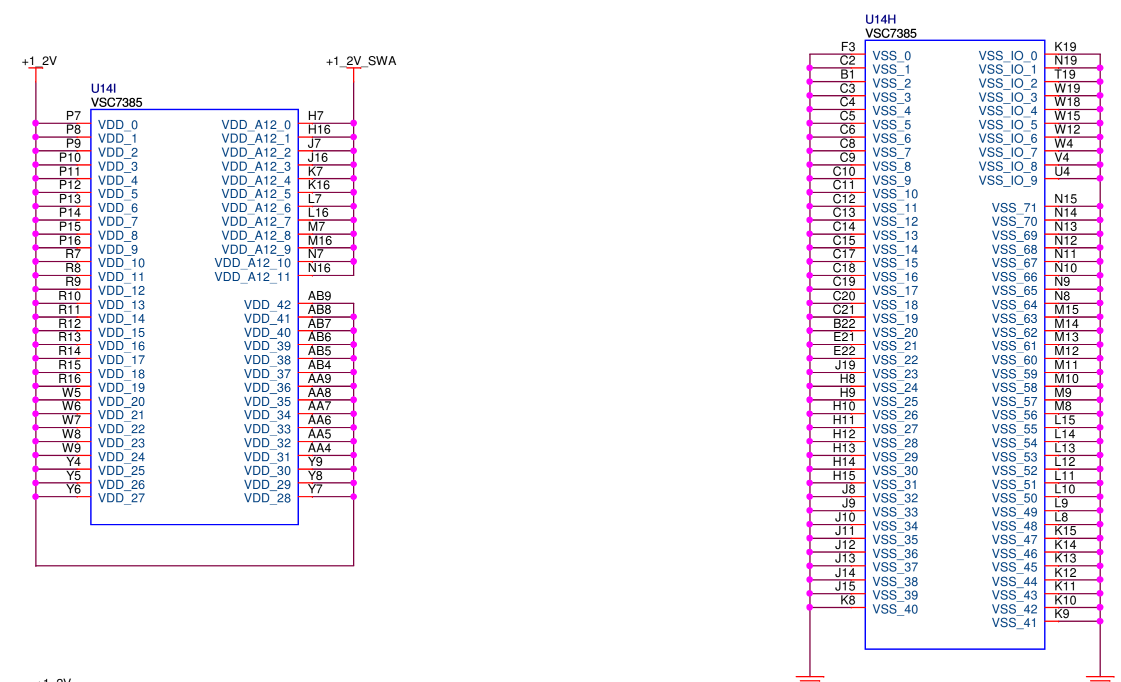
GIGABIT ETHERNET SWITCH INTERFACE

MAC INTERFACE SIGNALS

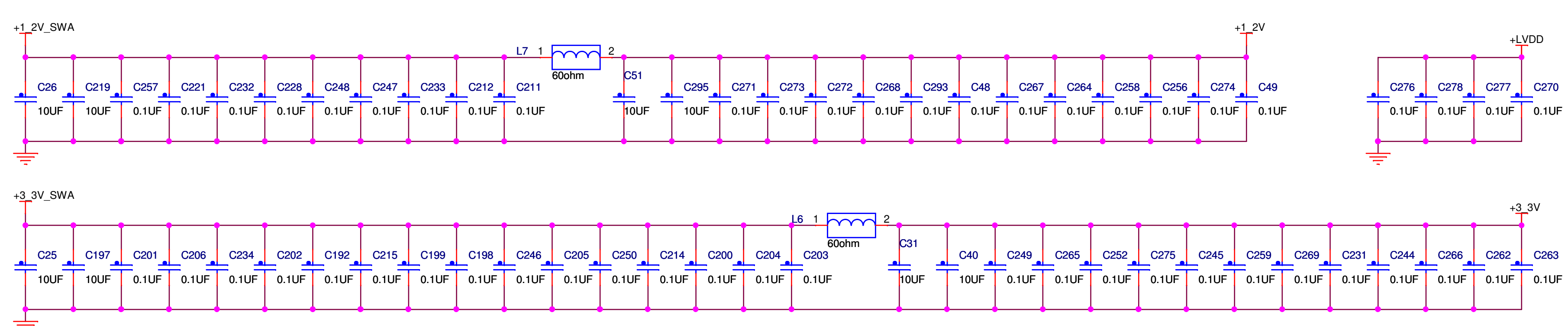


ETHERNET SWITCH POWER PINS



Power Supply Pins	Nominal Voltages	Associated Functional Pins
$VDDIO_{MAC}$	3.3V, 2.5V, 1.5V	TXD[3:0], TX_CTL, TX_CLK, RXD[3:0], RX_CTL, RX_CLK, TXREF_n, $CLK125_{MAC}$
$VDDIO_{micro}$	3.3V, 2.5V, 1.5V	SOFT_RESET, RESET, MDINT_n, MDIO, MDC, MICROREF, $CLK125_{micro}$
$VDDIO_{ctl}$	3.3V, 2.5V	TDI, TDO, TMS, TCK, TRST, EEDAT, EECLK
VDD33	3.3V	LED[4:0], CMODE[7:0], TXVN, TXVP, REF_REXT, REF_FILT, XTAL1

DECAPS FOR ETHERNET SWITCH



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ICAP Classification: FCP: ___ FIUO: <FIUO>PUBI: X

Drawing Title: **RDB for P1 and P2 devices**

Page Title: **Ethernet Switch**

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GIGABIT ETHERNET PORTS

RGMII (eTSEC3) and SGMII (eTSEC2) | SWITCH PORT 1 & 2 | SWITCH PORT 3 & 4

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ICAP Classification: FCP: ___ FIUO: <FIUO> PUBI: X

Drawing Title: **RDB for P1 and P2 devices**

Page Title: **Ethernet RJ-45 Ports**

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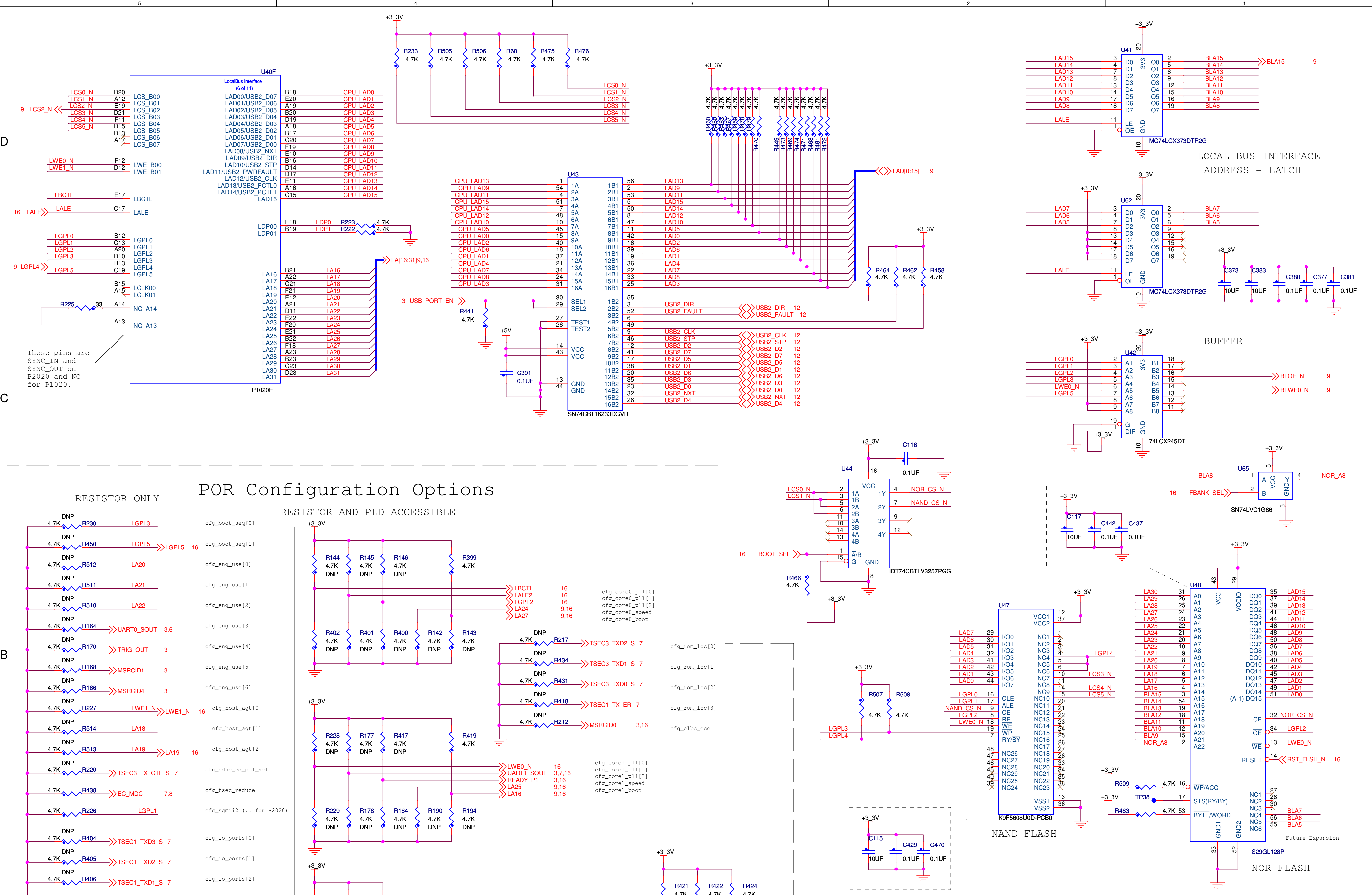

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ICAP Classification: FCP: ___ FIUO: <FIUO> PUBI: X

Drawing Title: RDB for P1 and P2 devices

Page Title: Local Bus and POR configs

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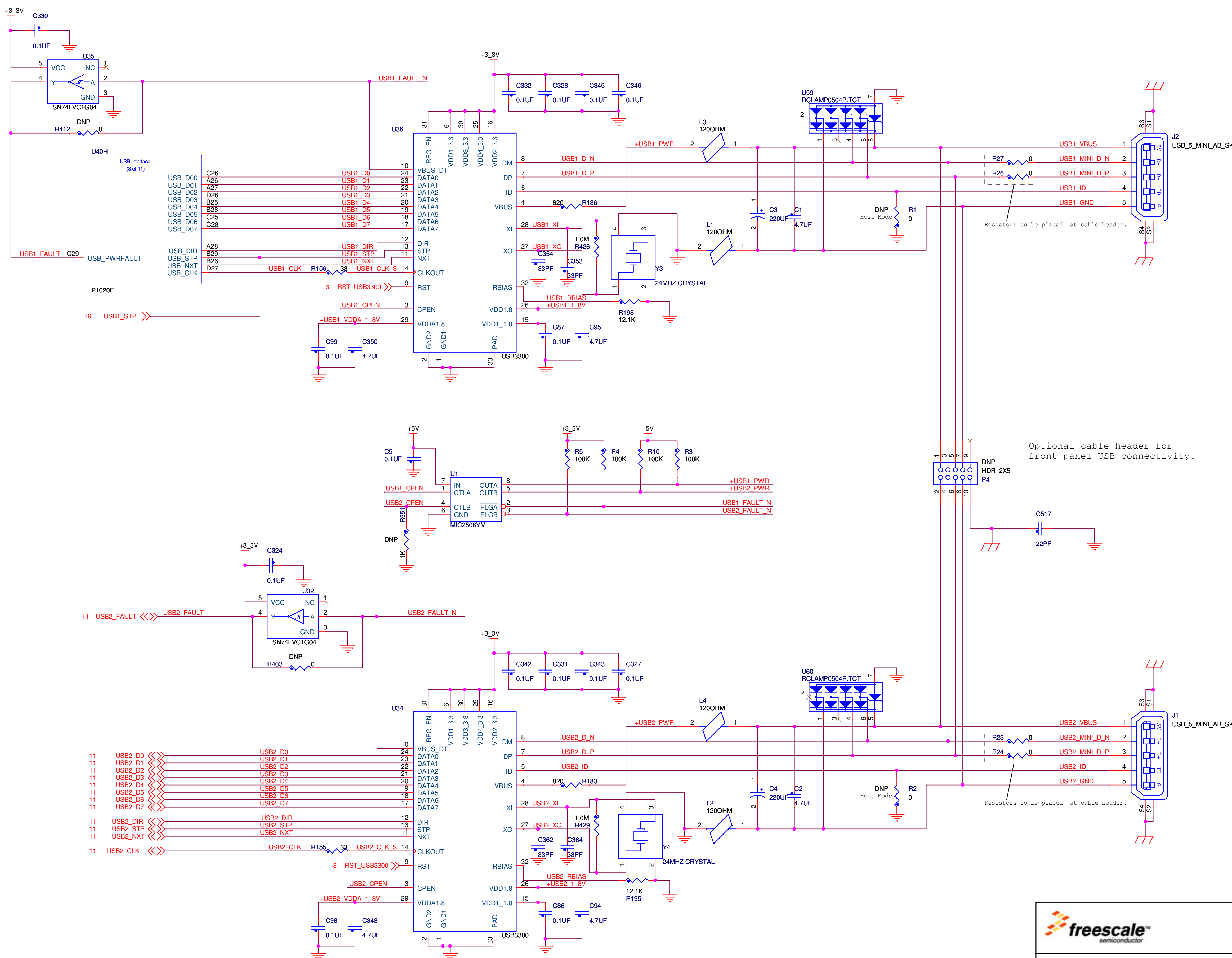
USB



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ICAP Classification: FCP: ___ FIUO: <FIUO>PUBI: X	
Drawing Title:	RDB for P1 and P2 devices
Page Title:	USB
Size: C	Document Number: SCH-26158 PDF: SPF-26158
Rev: D	
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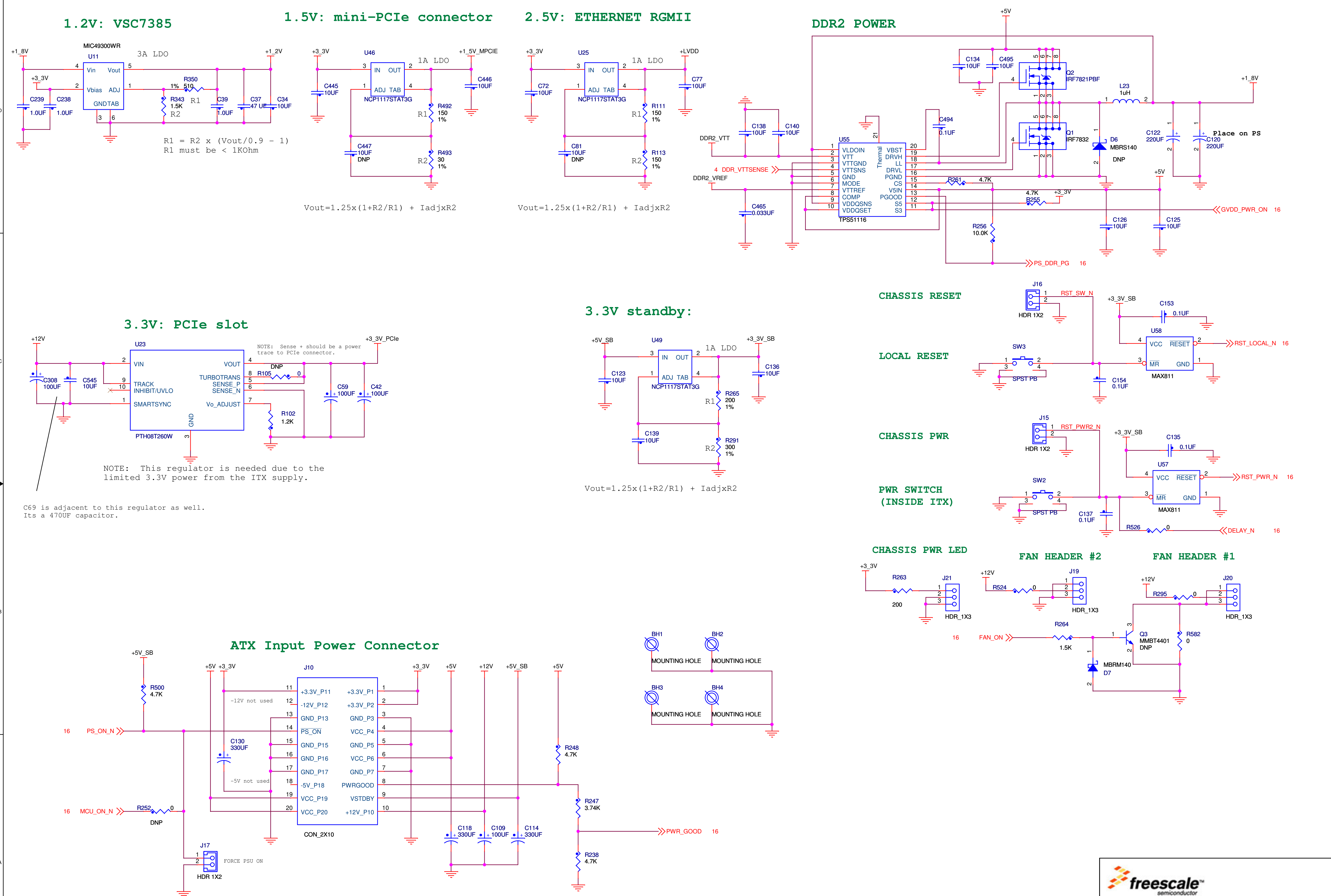

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ICAP Classification:	FCP: ___	FIUO: <FIUO>PUBI: X
Drawing Title:	RDB for P1 and P2 devices	
Page Title:	Misc Power & ITX Connections	
Size: C	Document Number: SCH-26158 PDF: SPF-26158	Rev: D
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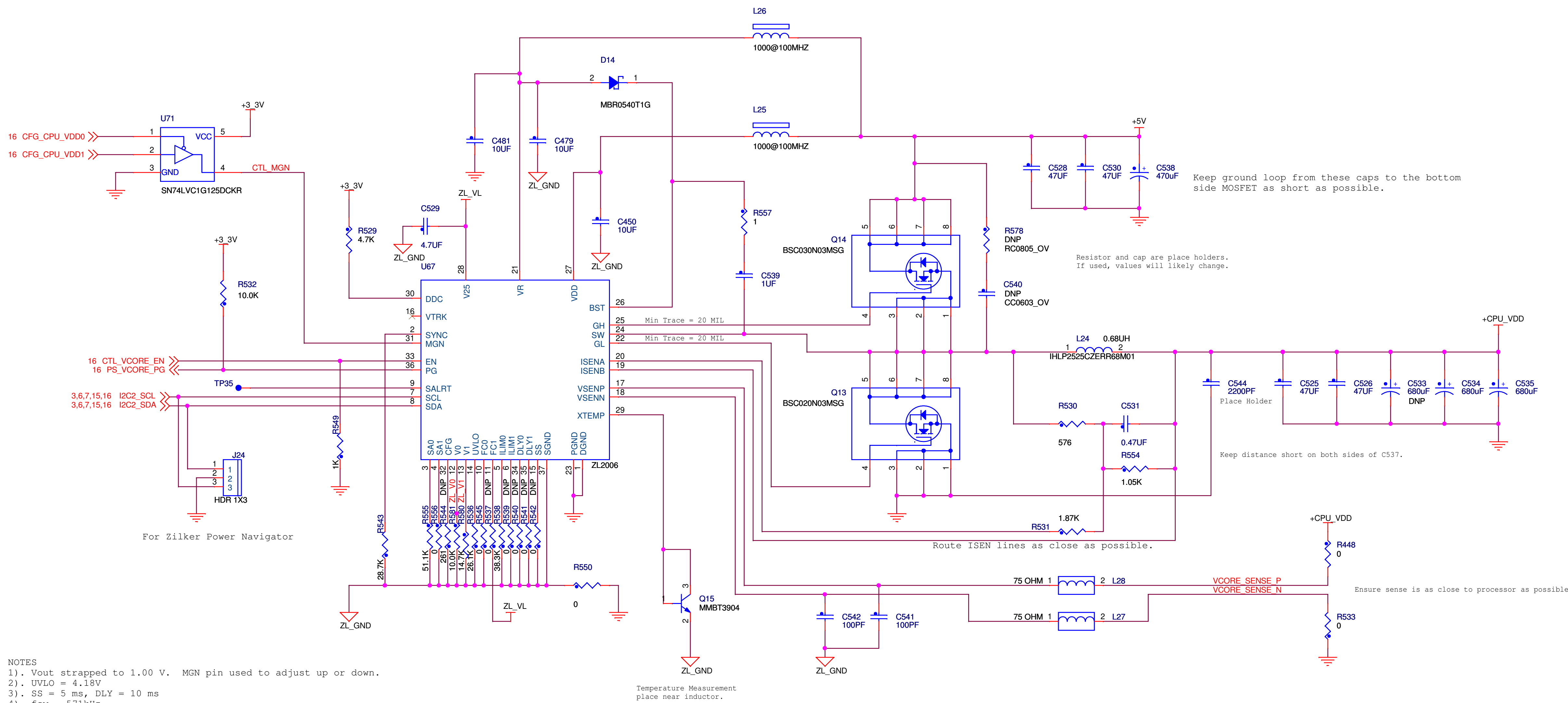
CPU VDD POWER

```
CFG_CPU_VDD[0:1] = b'01 => MGN high         VDD=1.05V    P2020 Devices
CFG_CPU_VDD[0:1] = b'00 => MGN low          VDD=0.95V    P1020 Devices
CFG_CPU_VDD[0:1] = b'1X => MGN tristated... VDD=1.00V    P1020 Devices (second option)
```



NOTES
1). Vout strapped to 1.00 V. MGN pin used to adjust up or down.
2). UVLO = 4.18V
3). SS = 5 ms, DLY = 10 ms
4). fsw = 571kHz
5). ILIM = 70mV / 5.5mohm = 12.7A
6). I2C ADDR = 0x11
7). CFG = AUTO DETECT

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ICAP Classification: FCP: ___ FIUO: <FIUO>PUBI: X

Drawing Title: **RDB for P1 and P2 devices**

Page Title: **VDD POWER SUPPLY**

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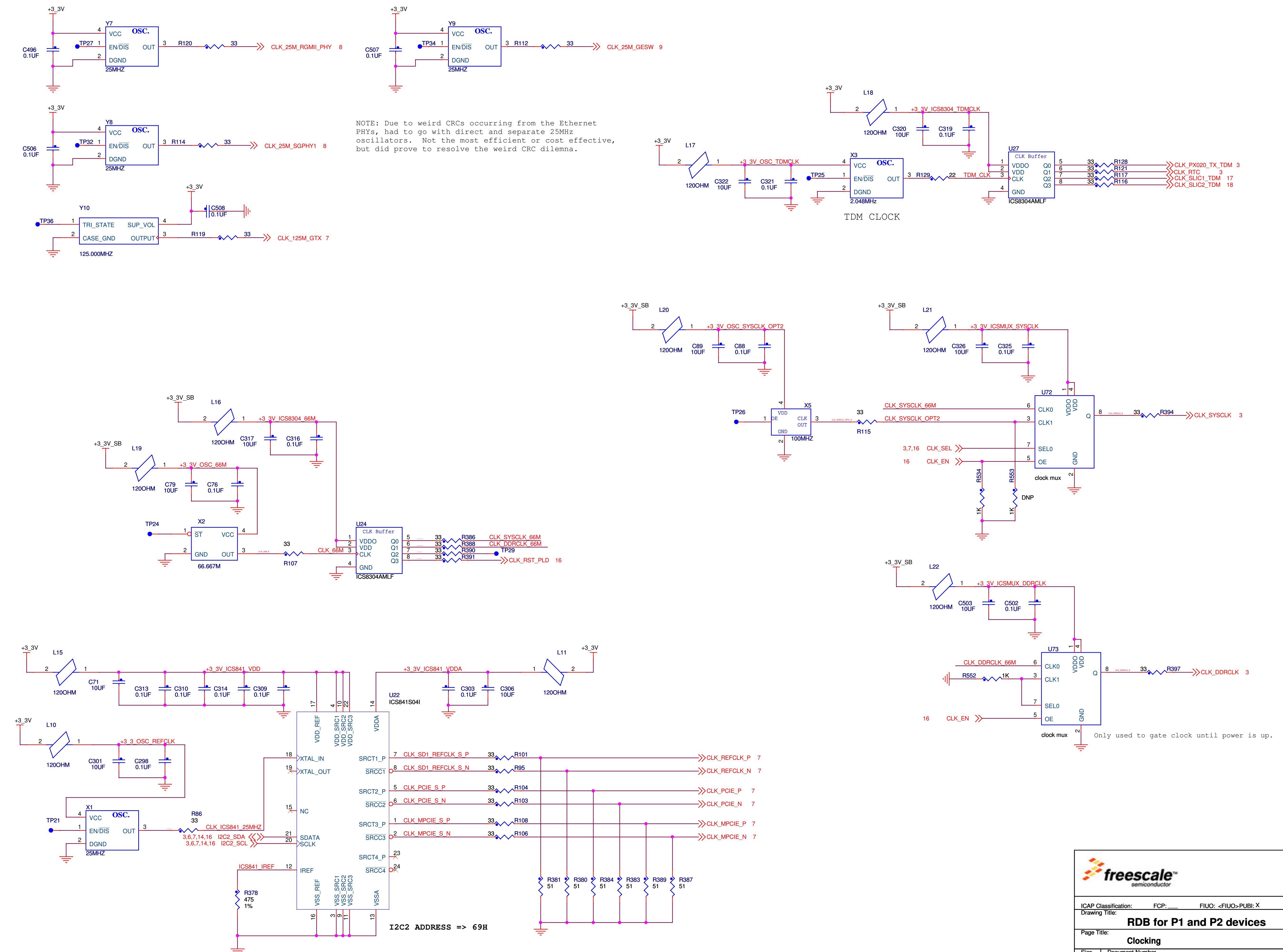

NOTE: Due to weird CRCs occurring from the Ethernet PHYs, had to go with direct and separate 25MHz oscillators. Not the most efficient or cost effective, but did prove to resolve the weird CRC dilemna.

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ICAP Classification: FCP: ___ FIUO: <FIUO>PUBI: X

Drawing Title: **RDB for P1 and P2 devices**

Page Title: **Clocking**

Size: C | Document Number: SCH-26158 PDF: SPF-26158 | Rev: D

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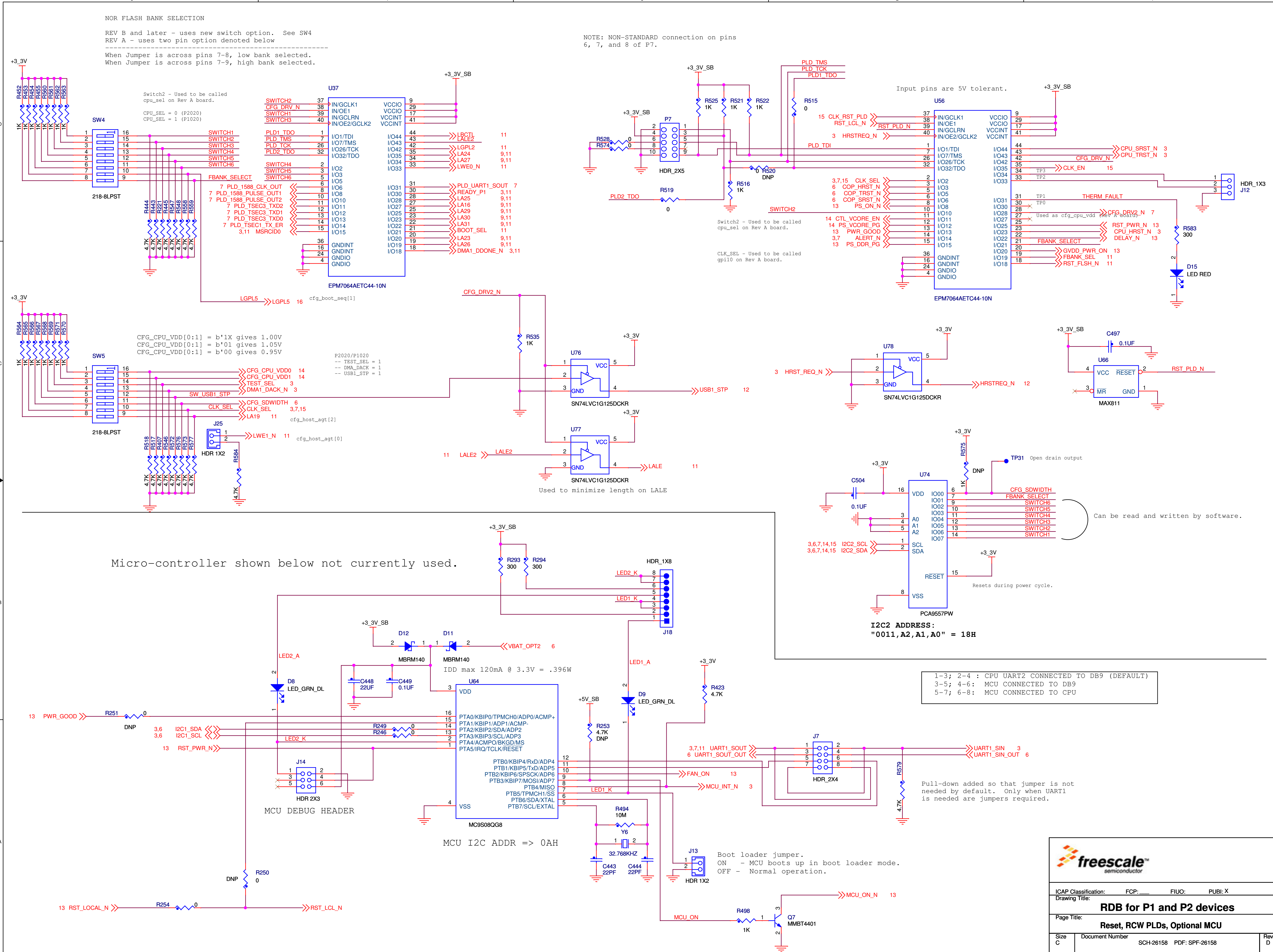

ICAP Classification: FCP: ___ FIUO: PUBI: X

Drawing Title: **RDB for P1 and P2 devices**

Page Title: **Reset, RCW PLDs, Optional MCU**

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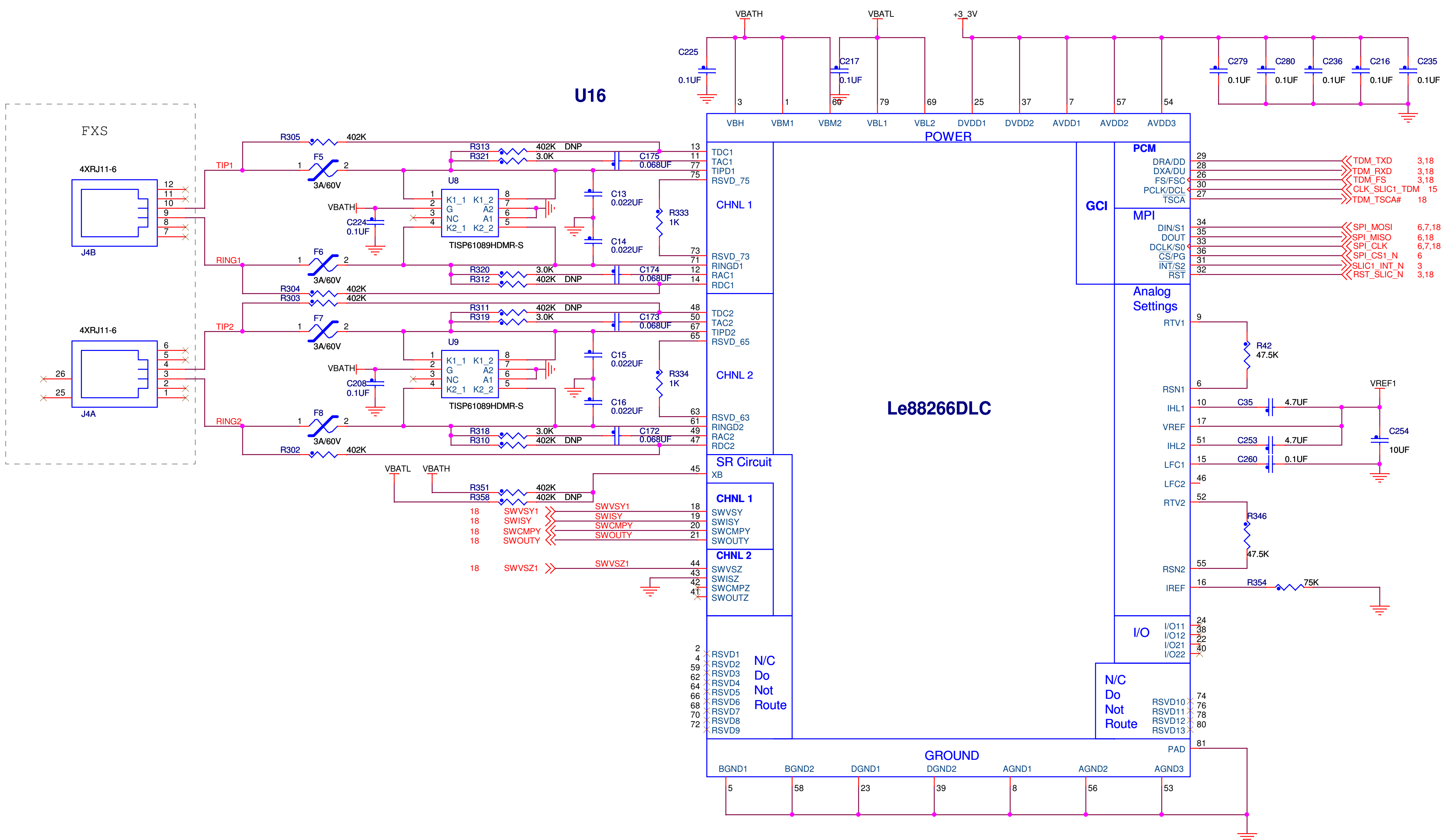
SLIC INTERFACE_1

VOICE PORT 1 & 2



This sheet is only applicable for devices that have a TDM Port. For example, P1020.
TDM Port not Available for P2020

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ICAP Classification:	FCP: ___	FIUO:	PUBI: X
Drawing Title:	RDB for P1 and P2 devices		
Page Title:	SLIC INTERFACE 1		
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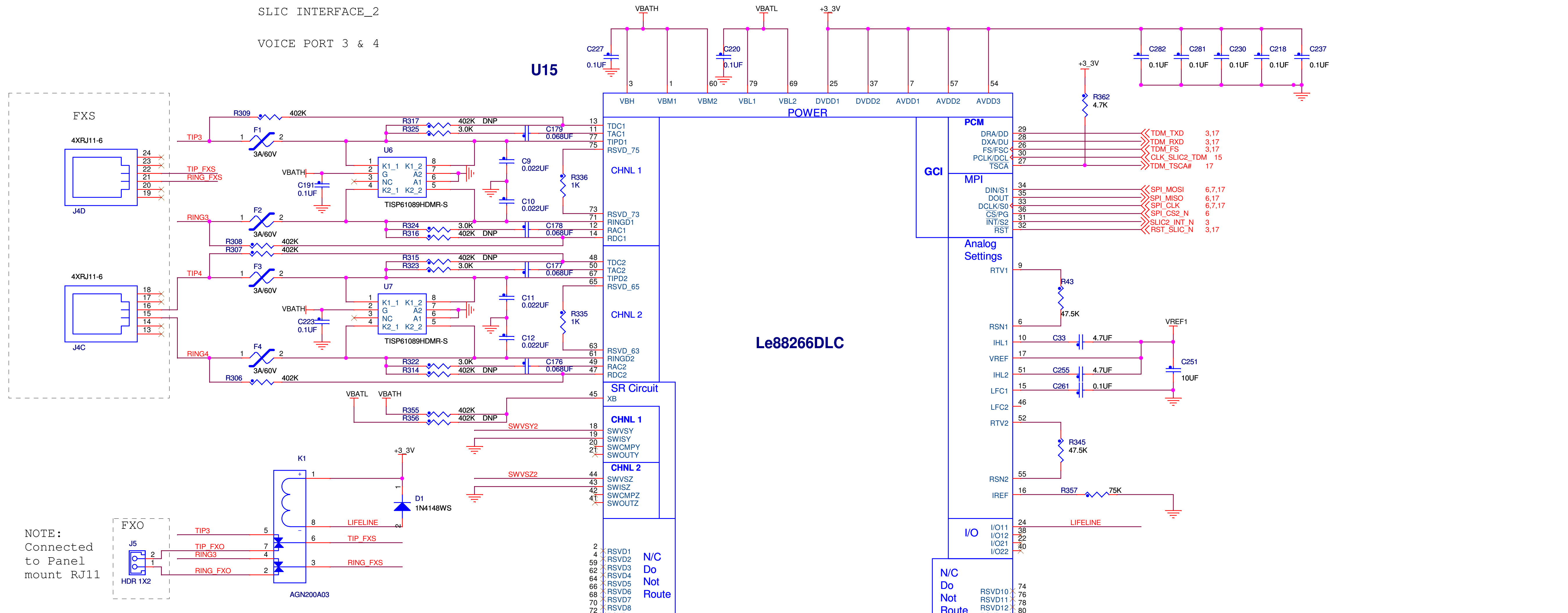
SLIC INTERFACE_2

VOICE PORT 3 & 4

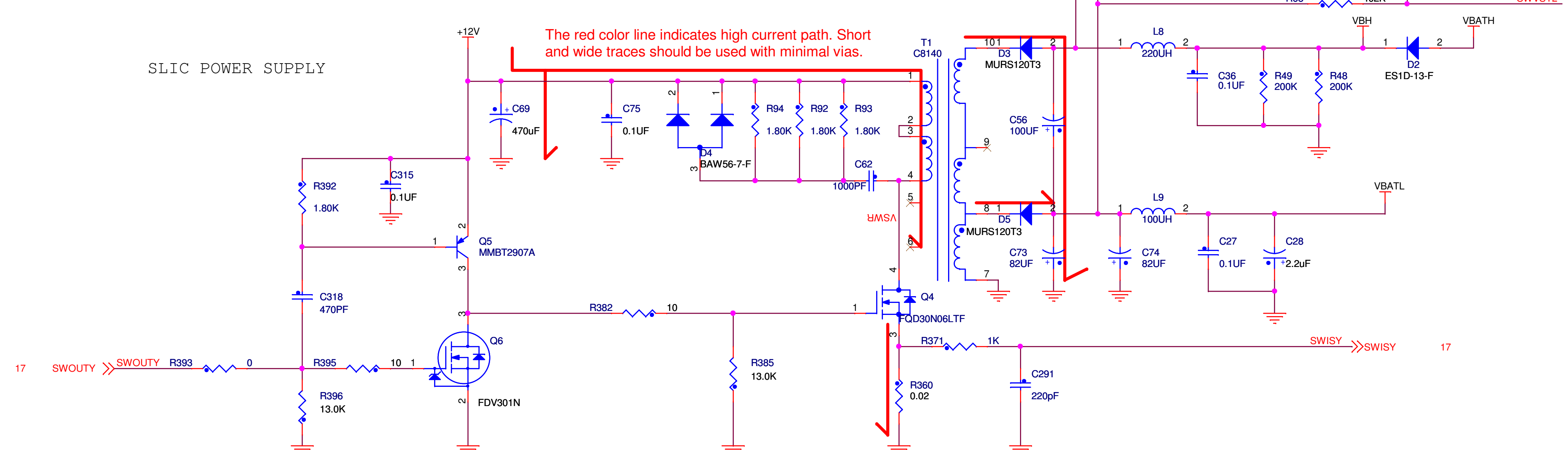


RELAY STATE

STATE	TIP_FXS Connected to	RING_FXS Connected to
ENERGIZED	TIP4 (FXS)	RING4 (FXS)
DEENERGIZED	TIP_FXO	RING_FXO

This sheet is only applicable for devices that have a TDM Port. For example, P1020.
TDM Port not Available for P2020

SLIC POWER SUPPLY



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ICAP Classification: FCP: ___ FIUO: PUBI: X

Drawing Title: RDB for P1 and P2 devices

Page Title: SLIC INTERFACE 2

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